Silicon Nanoelectronics

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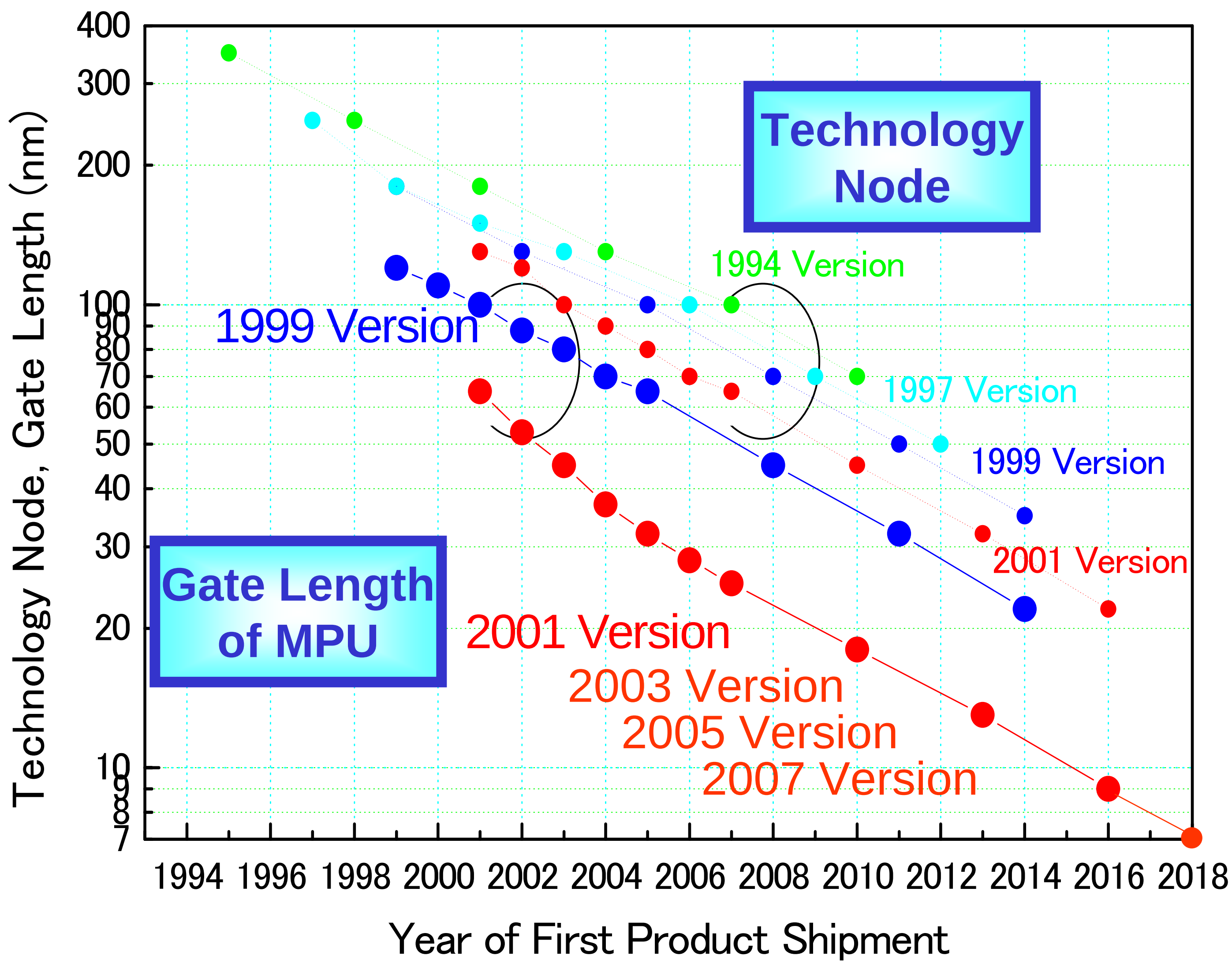
1. **Introduction: Rapid Miniaturization**
2. **Future Silicon Nanoelectronics**
   --- More Moore, More Than Moore, and Beyond CMOS
3. **CMOS Extension**
   2.1. New transistor structures and new materials
   2.2. Variability
4. **Single-Electron Transistors (Beyond CMOS)**
5. **Summary**

CMOS Scaling (ITRS Roadmap)



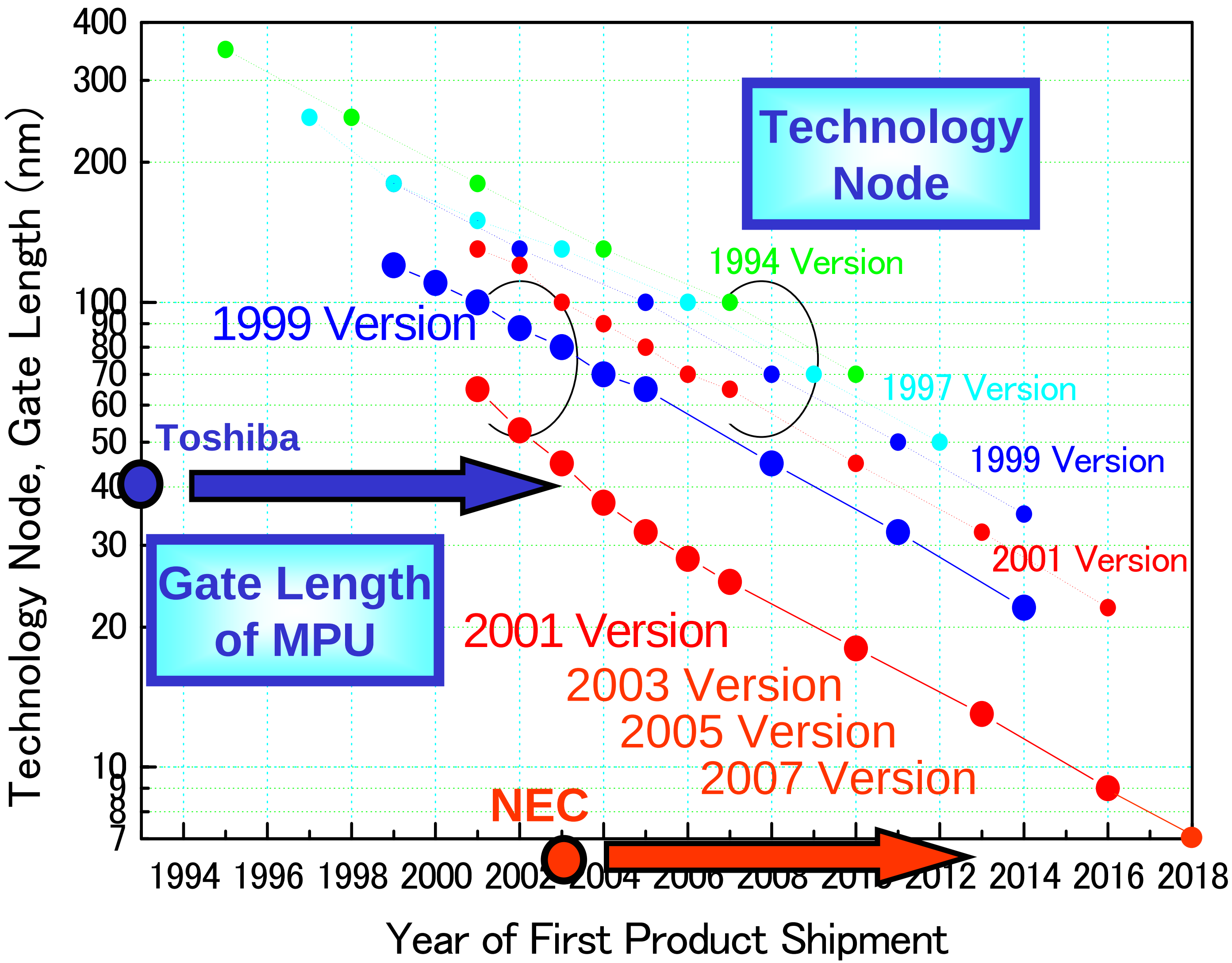
The Smallest Devices in Research

- 10 nm Scale Devices in Conferences

Dec. 1993	Toshiba	40nm NMOS	Bulk
Dec. 2000	Intel	30nm CMOS	Bulk
June 2001	Intel	20nm CMOS	Bulk
Dec. 2001	STMicro	16nm NMOS	Bulk
Dec. 2001	AMD	15nm CMOS	Bulk
Dec. 2002	Toshiba	15nm CMOS	Bulk
Dec. 2002	IBM	6nm PMOS	PD SOI
Dec. 2003	NEC	5 nm CMOS	Bulk
June 2004	TSMC	5 nm CMOS	FinFET
June 2006	KAIST	5nm CMOS	GAA

- Silicon MOSFET is already in nano-scale!
- This is certainly a nanotechnology.

ITRS (Roadmap)



2. Future Silicon Nanoelectronics

--- More Moore, More Than Moore, and Beyond CMOS ---

Integrated Nanoelectronics

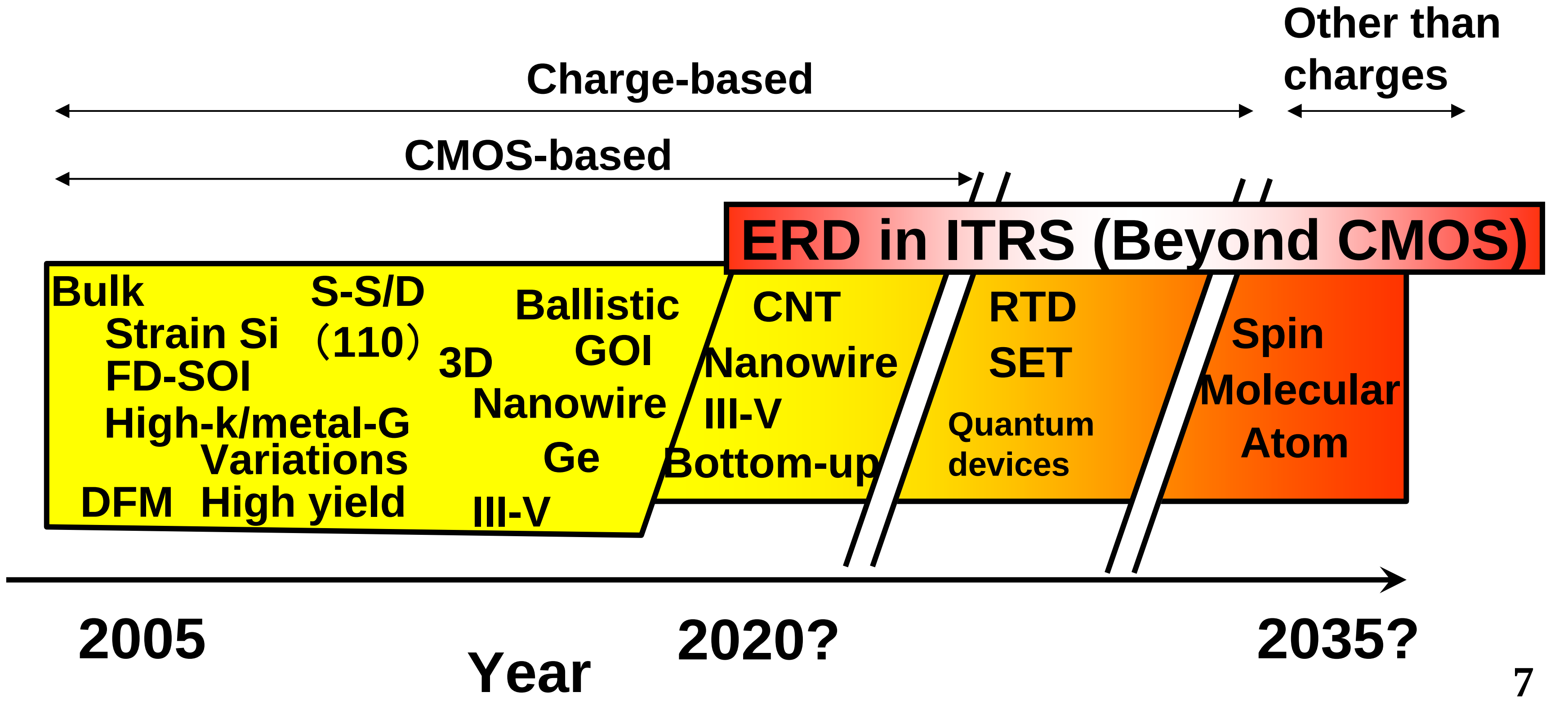
Three Important Elements for Nanoelectronics

1. Transistor (Information Processing)
2. Memory (Information Storage)
3. Interconnect (Information Transfer)

Transistors (Information Processing)

Information Processing Devices

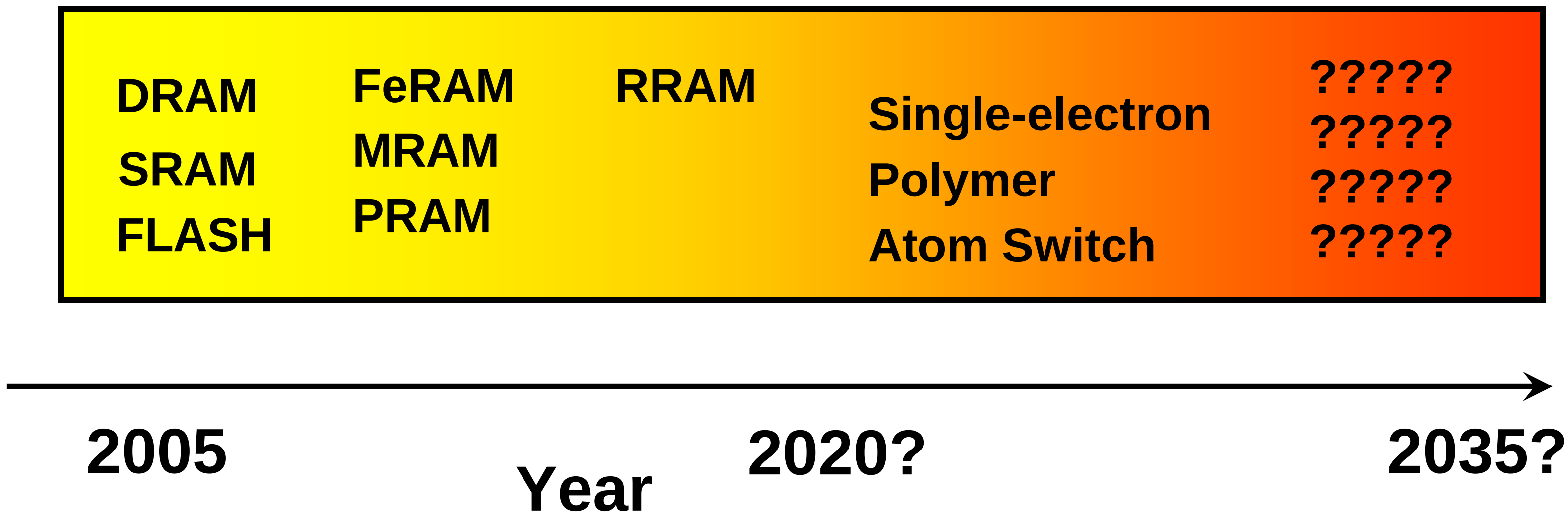
- No better device other than CMOS in “charge-based”. CMOS extension will be the most important.
- CNT-FET will also be classified to “CMOS Extension”.



Memories

Memory and Storage Devices

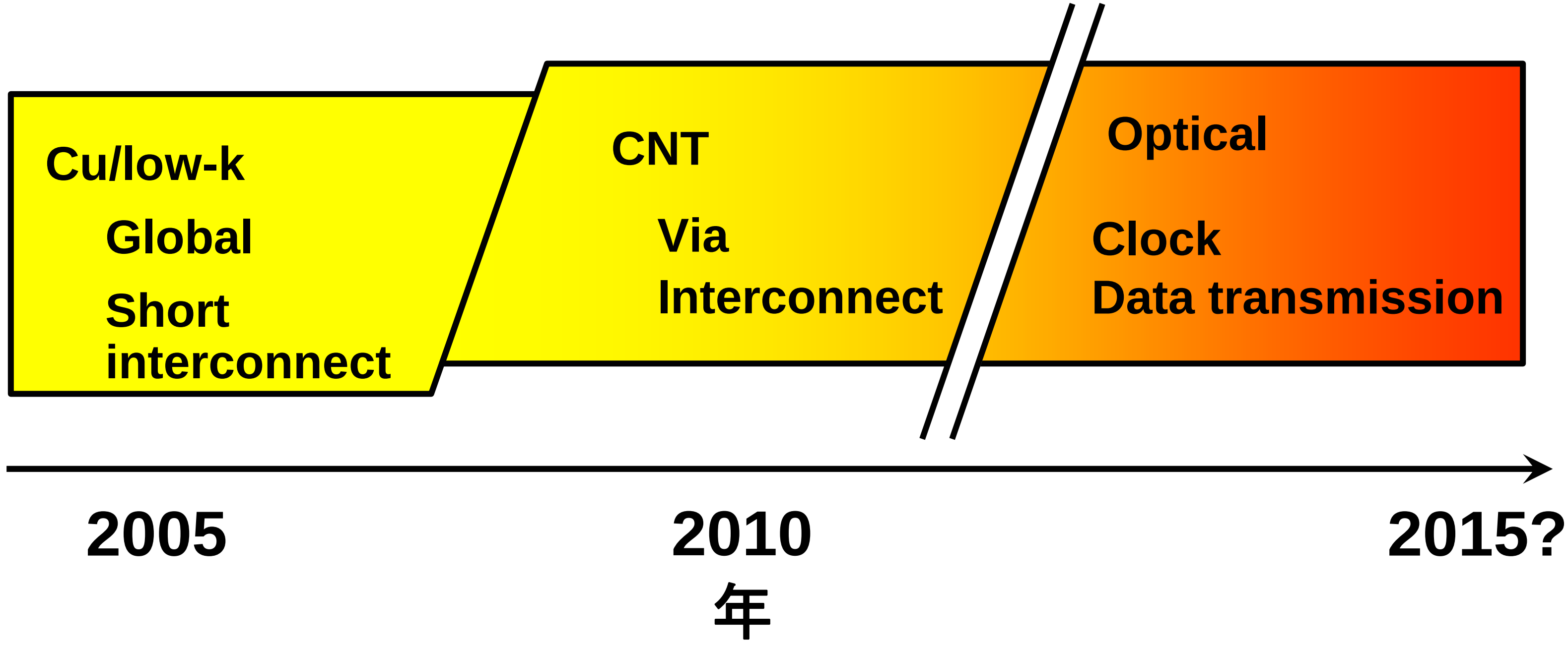
- New materials and nano-structures only for memory cells
  Other circuits are based on conventional CMOS
- A good example of fusion of new technology and CMOS



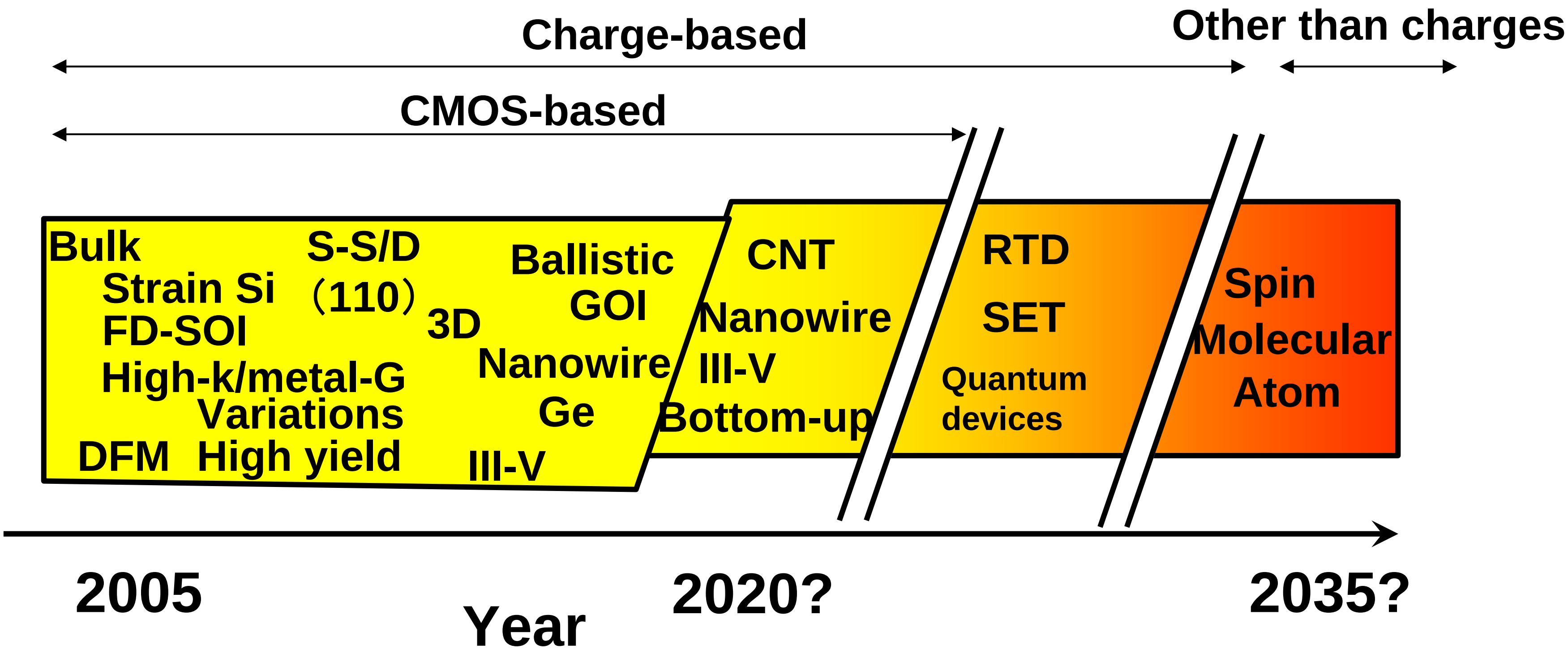
Interconnect Technology

Information Transfer

- No promising technology beyond Cu/low-k.
- Paradigm shift will happen earlier than transistors?
- Bottom up fabrication : CNT vias and interconnect
- New information transfer: Optical interconnect



Three Stages in Silicon Nanoelectronics

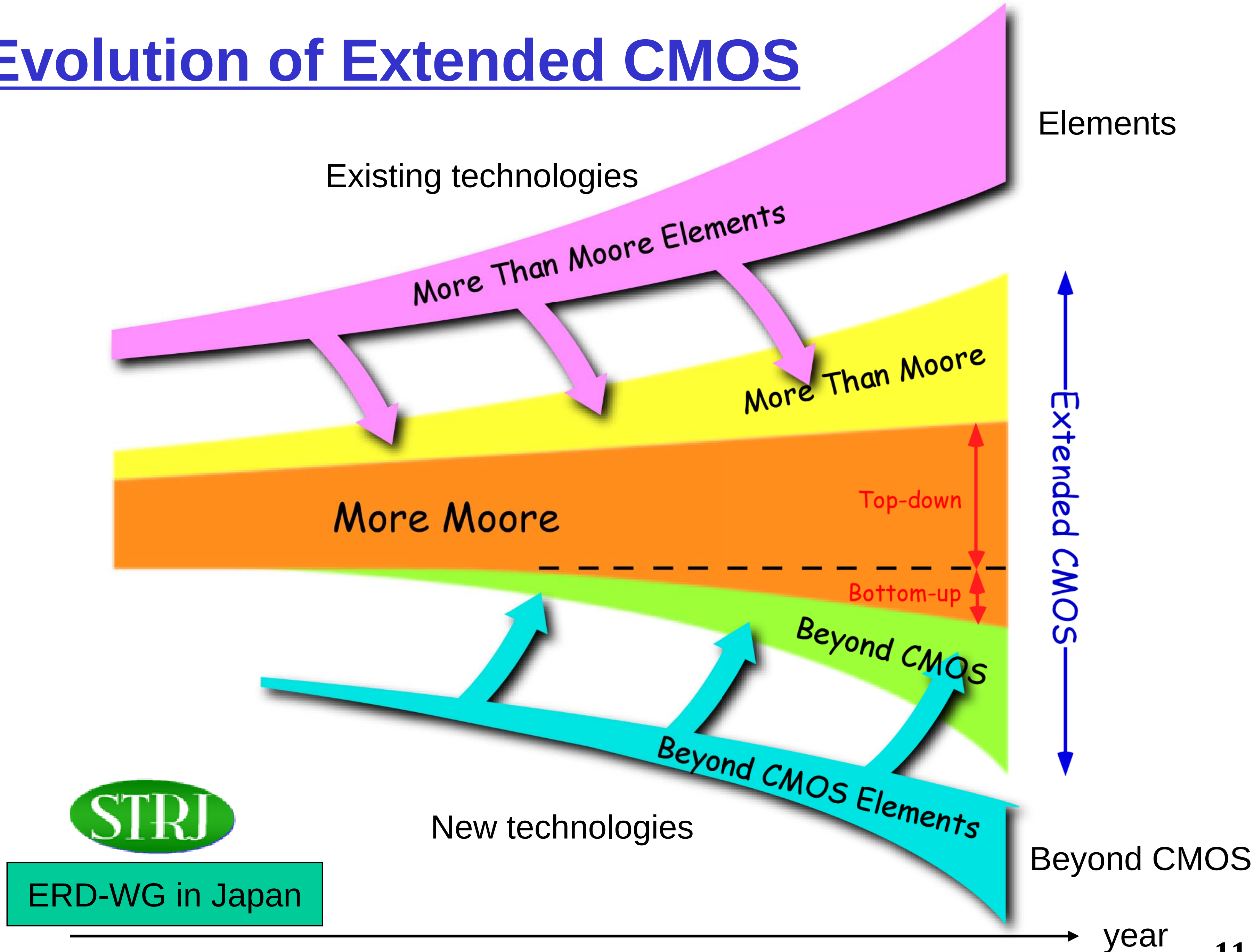


1. CMOS Extension
(More Moore)

3. Beyond CMOS

2. New Functions Added to CMOS
(More Than Moore)

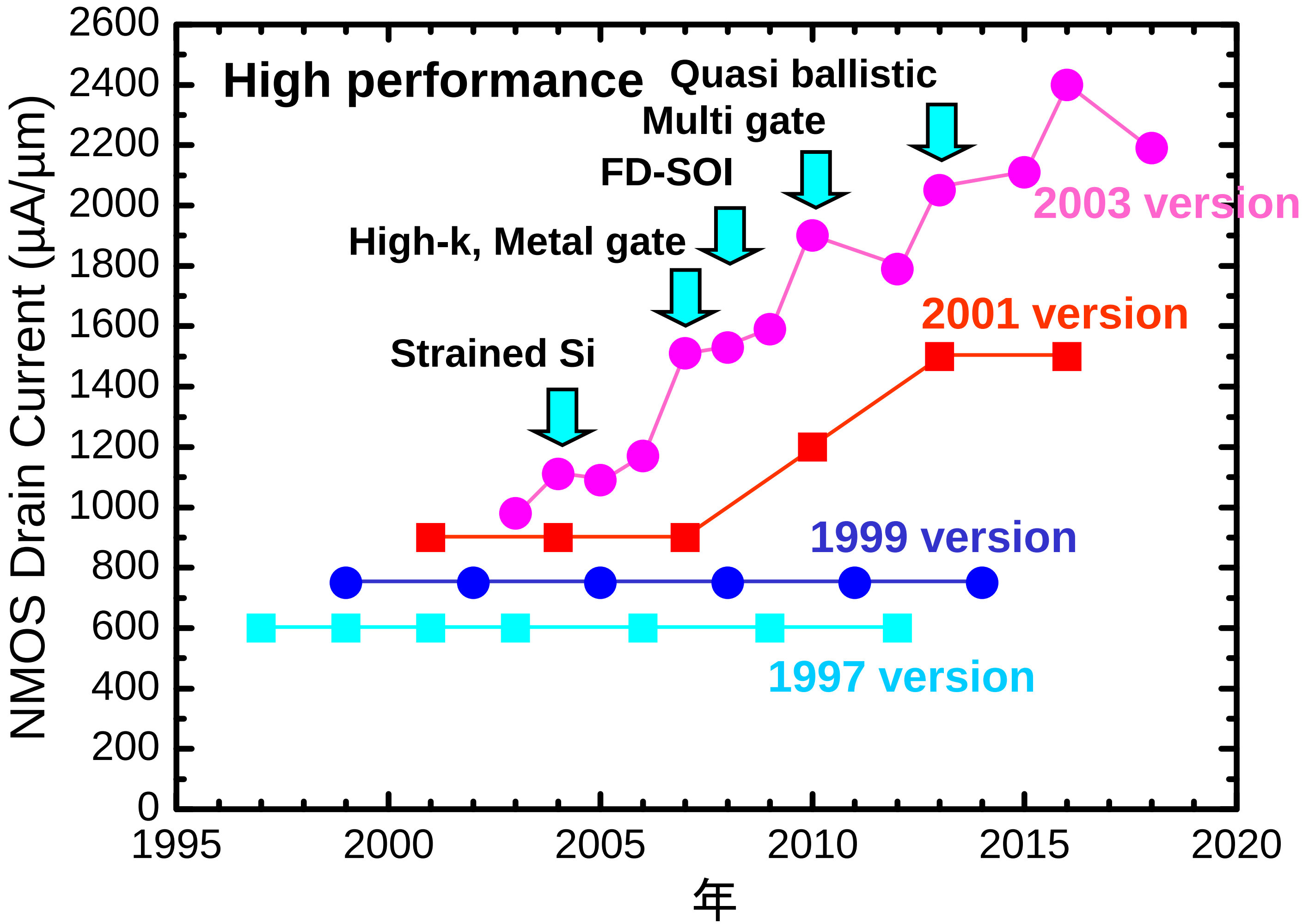
Evolution of Extended CMOS



3. CMOS Extension

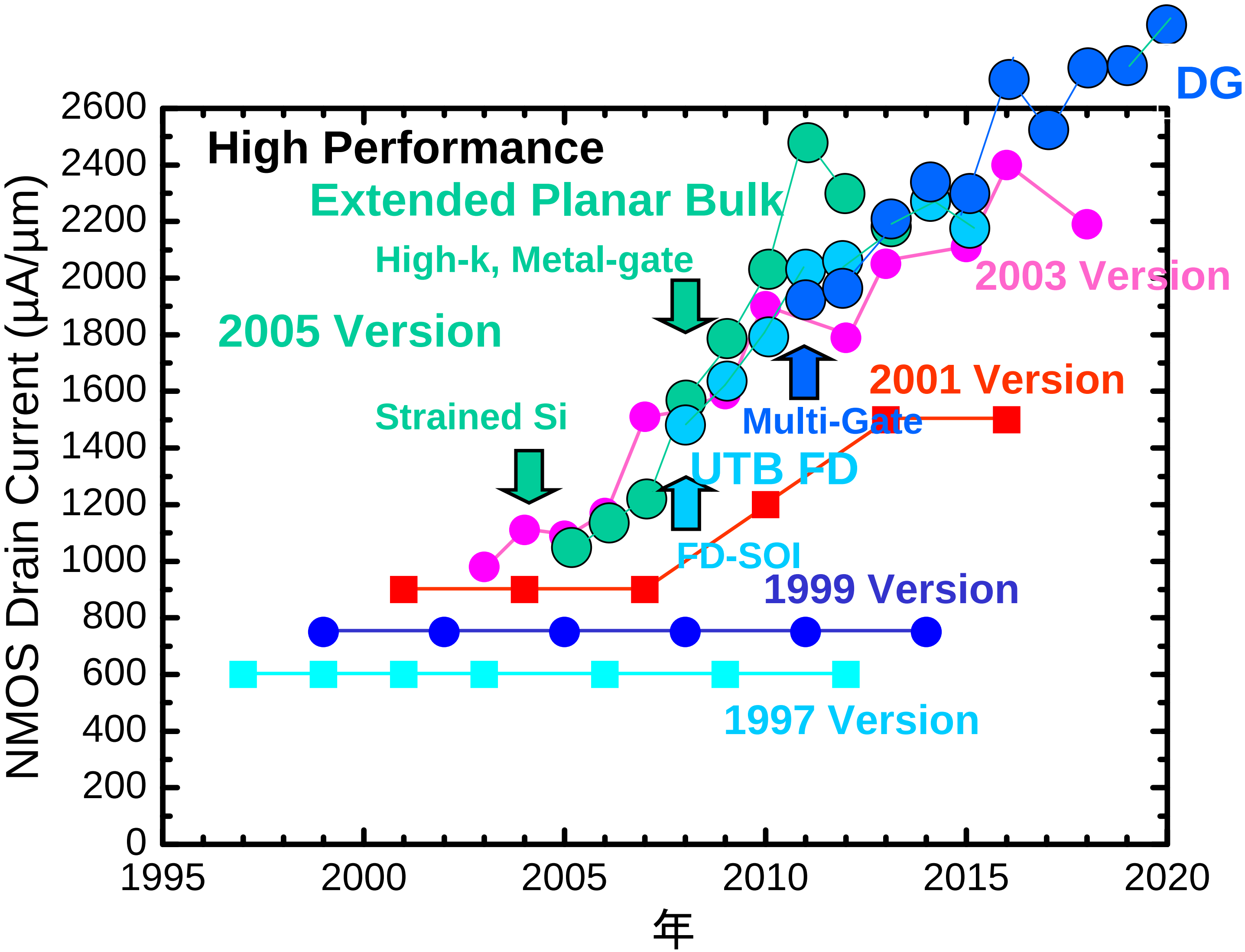
3.1. New transistor structures and new materials

Trend of Targeted Ion in ITRS

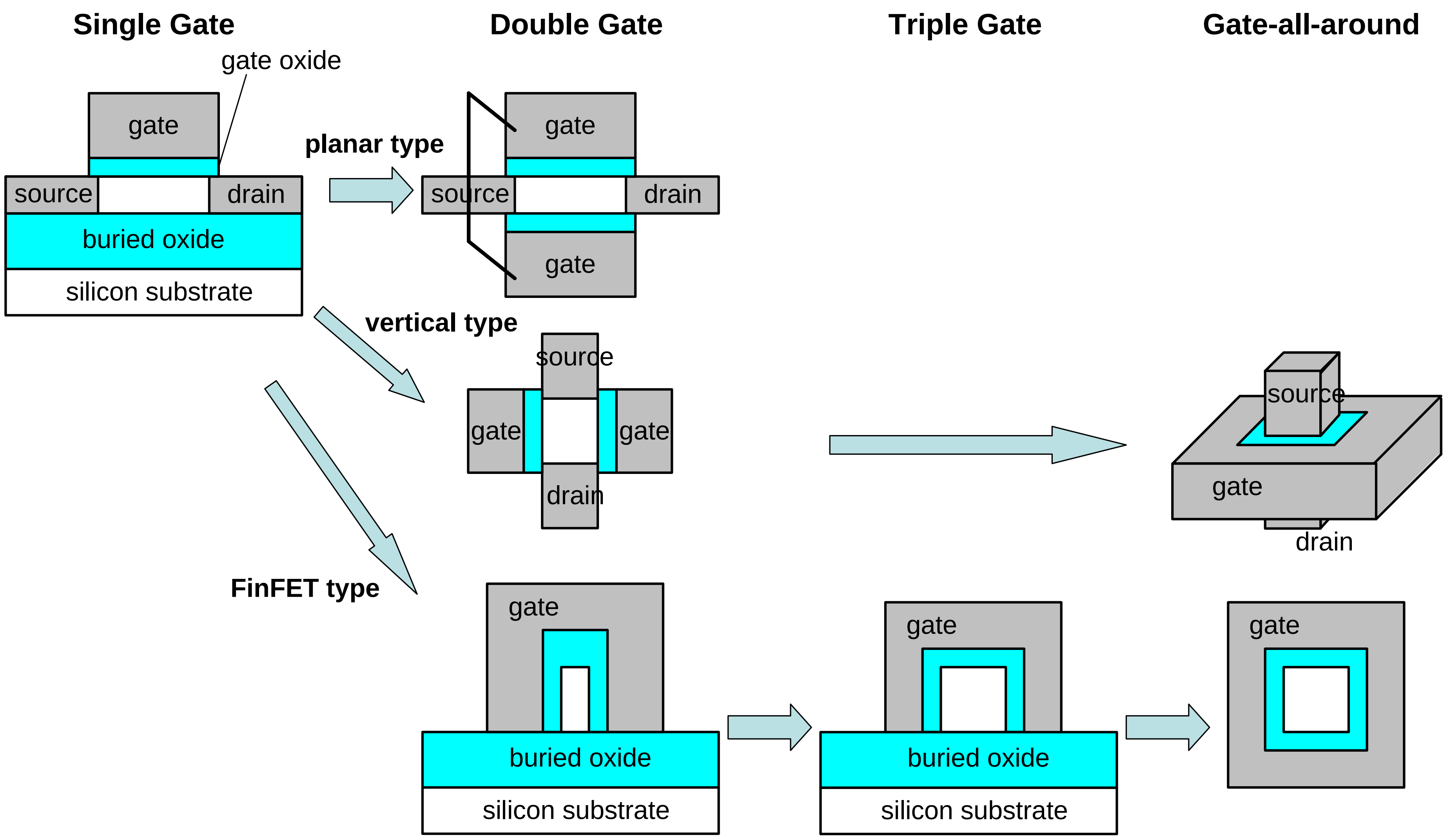


2003 ITRS, PIDS

On-Current in 2005 ITRS



Evolution of Transistor Structures

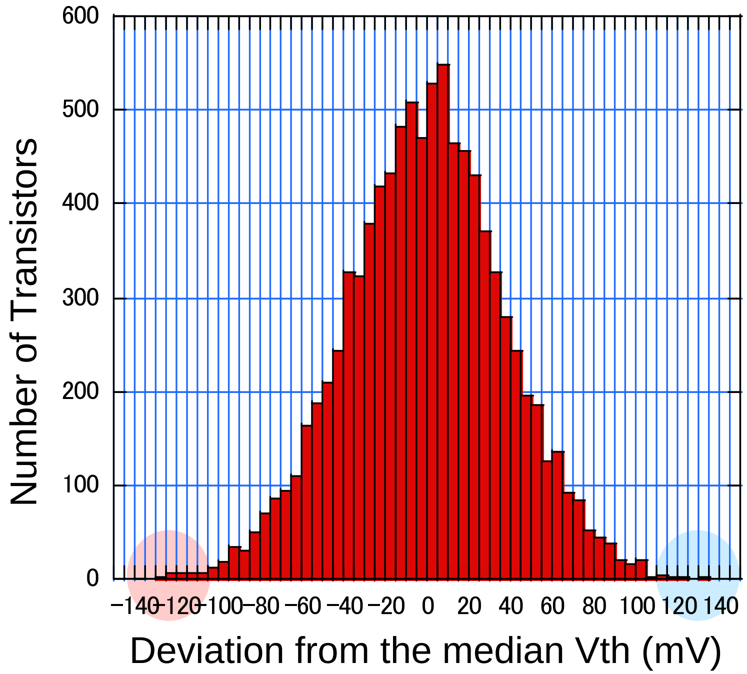


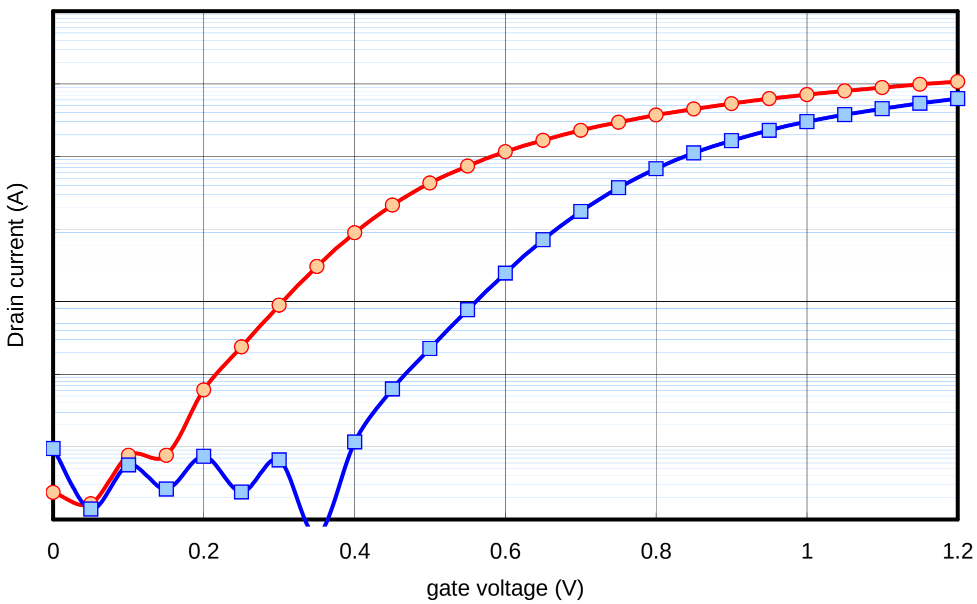
T. Hiramoto, IEICE Transactions on Electronics, vol. E90-C, p. 836, 2007.

3. CMOS Extension

3.2. Variability

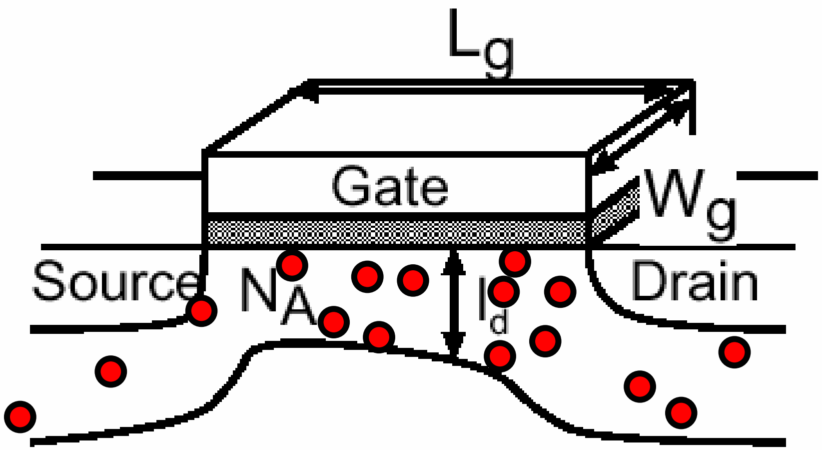
Example of Variations





Threshold voltage varies in wafer.

Statistic Distribution of Impurities



$$n = L_g W_g N_A l_d \qquad \sigma n = \sqrt{n}$$

$$\frac{\Delta N_A}{N_A} = \frac{\sqrt{n}}{n} = \frac{1}{\sqrt{n}}$$

$$\sigma V_{th} \propto \frac{t_{ox} N_A^{1/4}}{\sqrt{L_g W_g}}$$

The number of impurities follows the Poisson Distribution.

This simple equations neglect the impurity position distribution or percolation conduction.

$1/k \cdot k^{1/4}$

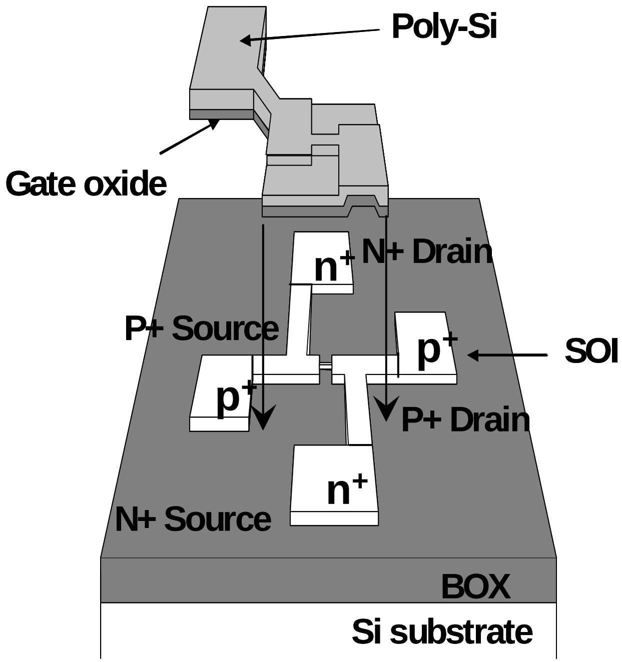
$1/k$

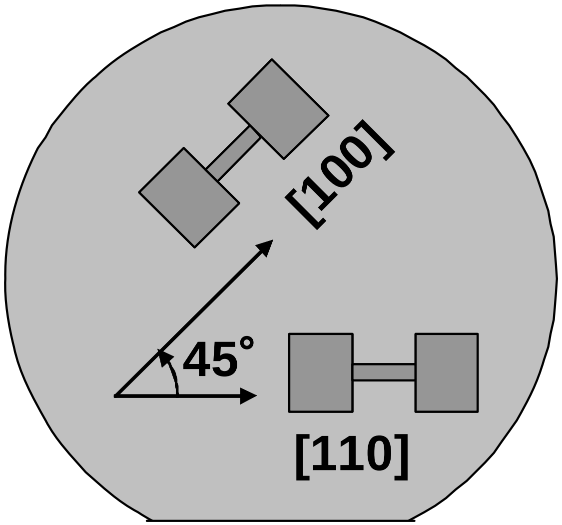
- Increases by $k^{1/4}$.

T. Mizuno et al. VLSI Tech. Symp. 1993.

New Type of Variability

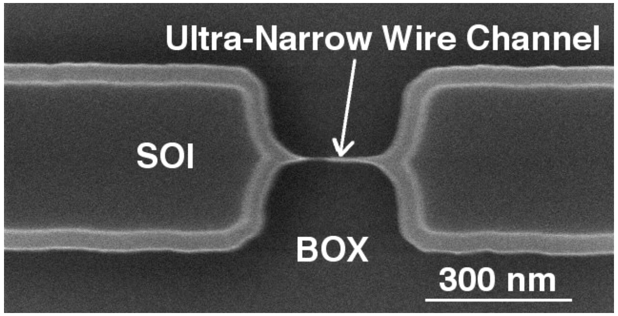
Silicon Nanowire FETs

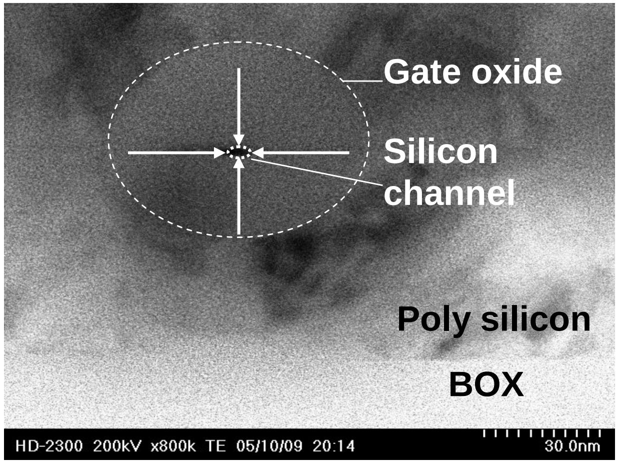




(100) wafer

Two channel directions

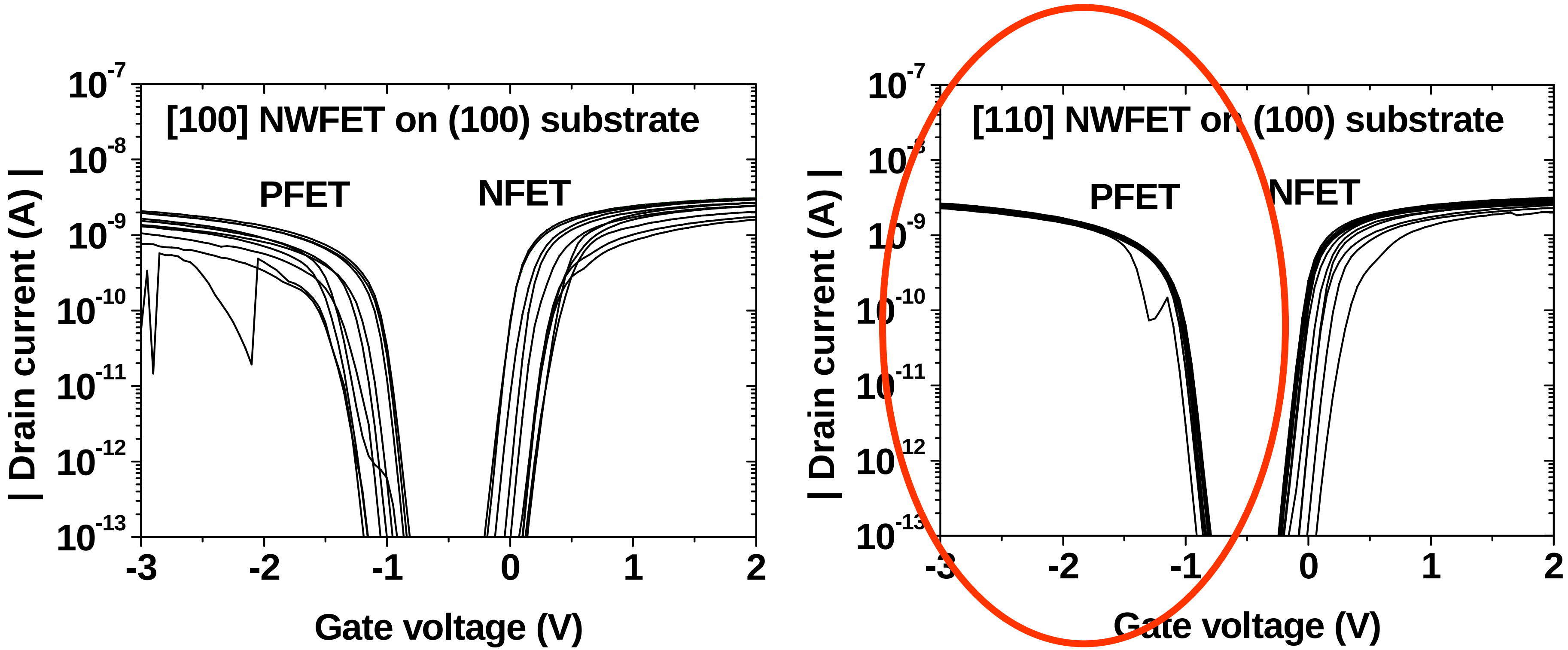




Both n-type and p-type operations in the same device.

M. Kobayashi and T. Hiramoto, IEDM, p. 1007, 2006.

Variations in nanowire FETs



Slight variations of channel width cause large Vth variation due to quantum confinement effect.

M. Kobayashi and T. Hiramoto, IEDM, p. 1007, 2006.

Robust Transistor Design Program

Robust Transistor Design

Term: 2006 – 2007
Headed by T. Hiramoto
In framework of MIRAI Project supported by NEDO

- **Characterization of Variations of Electrical Properties**
- **Characterization of Variations of Physical Parameters**

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- **Integrated Analysis of Variations**

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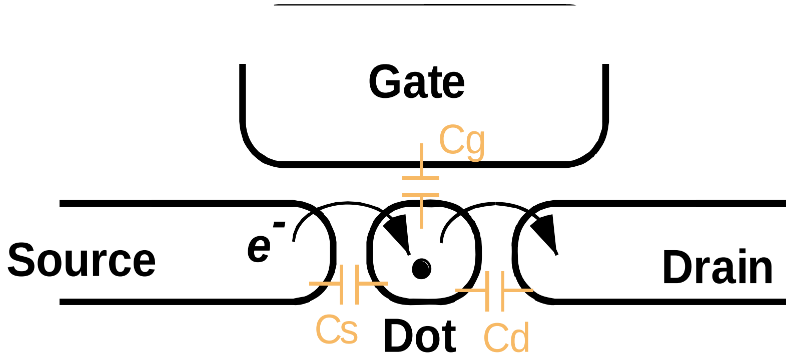
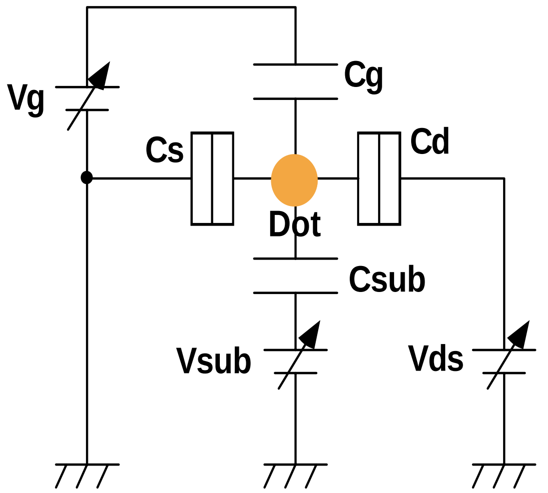
- **Physical Modeling of Variations and Applications to DFM**
- **Design of Transistors Robust to Variations**

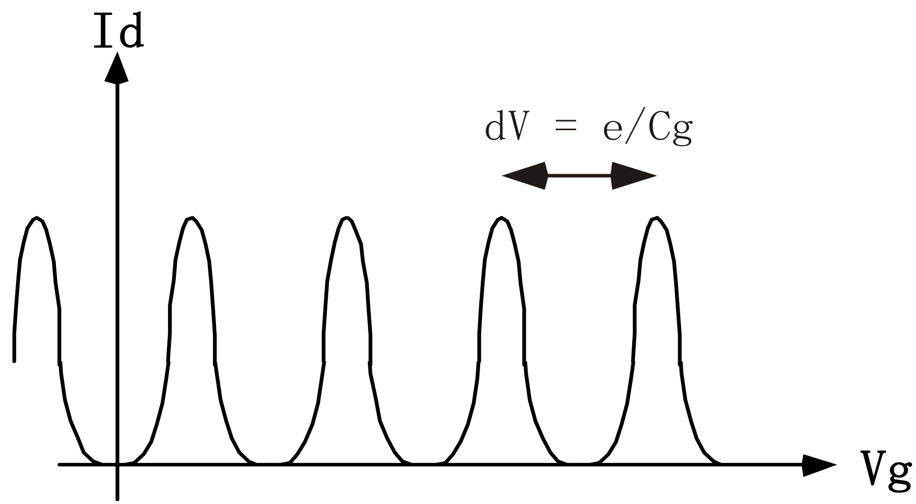
4. Beyond CMOS

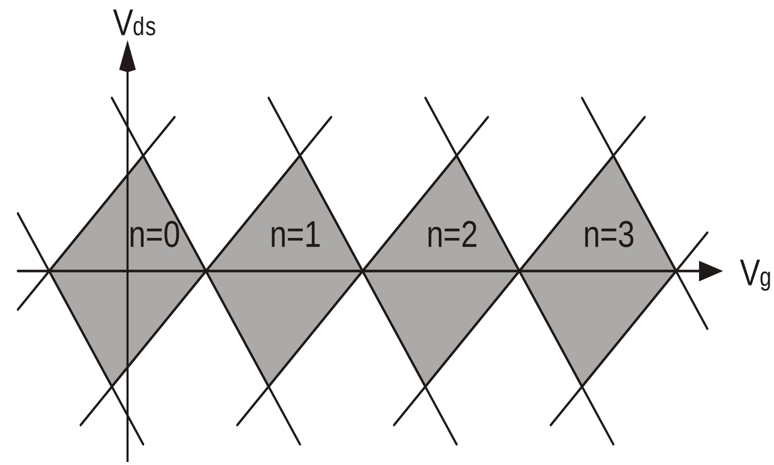
Single-Electron Transistors

Single-Electron Transistor (SET)





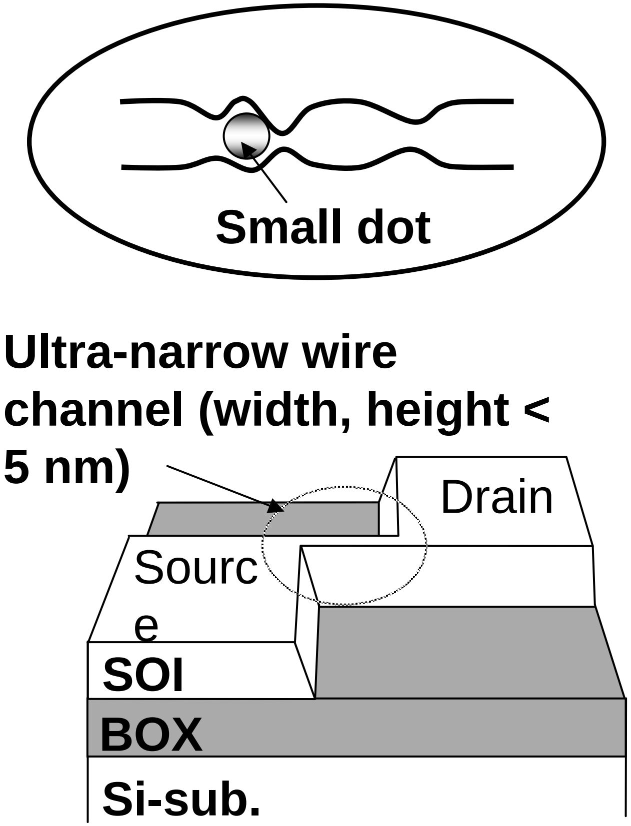


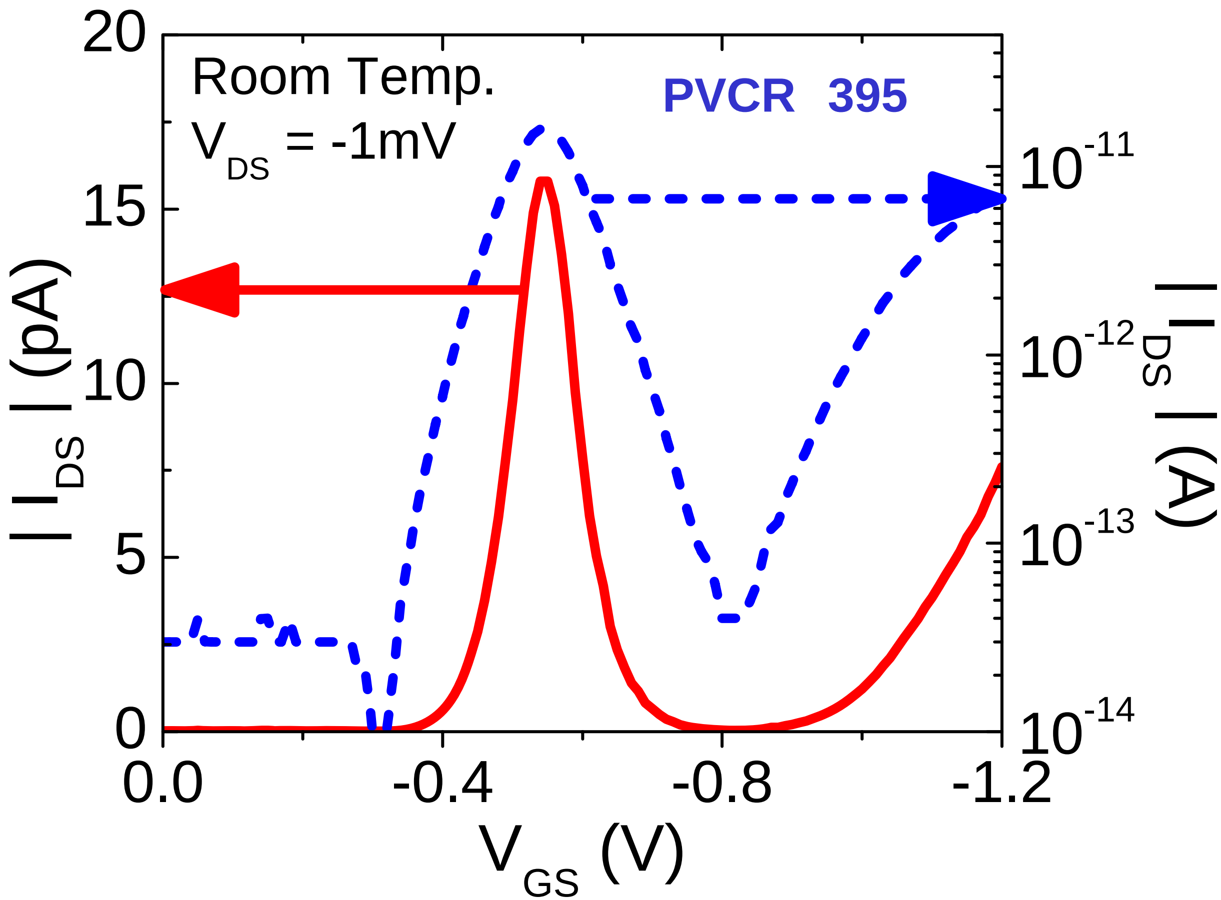


Charging Energy Ec = e^2/C_{total}

Temperature T < Ec (Ec ~ 26 meV when d ~ 10 nm)

Larger CB Oscillations at RT

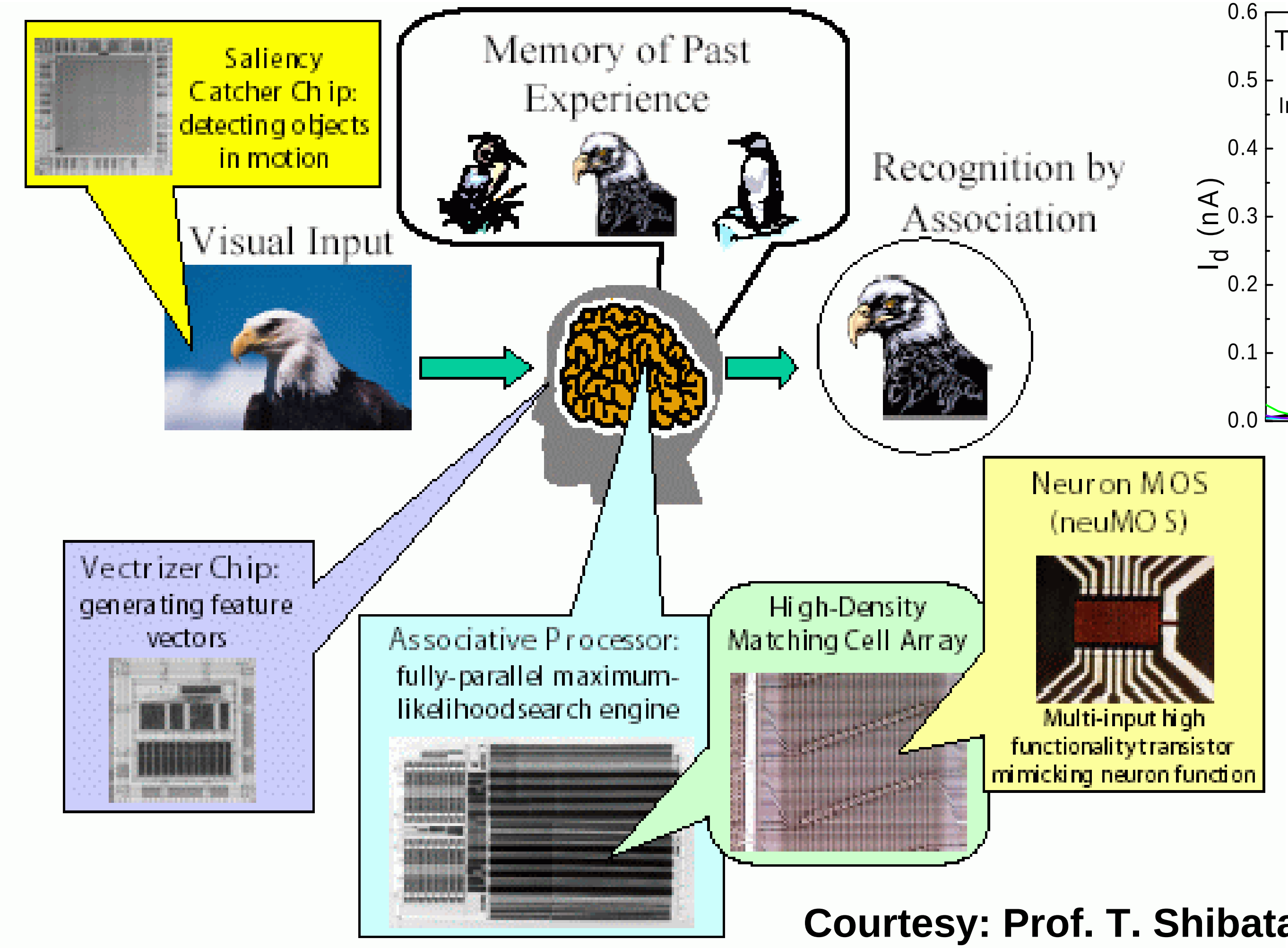


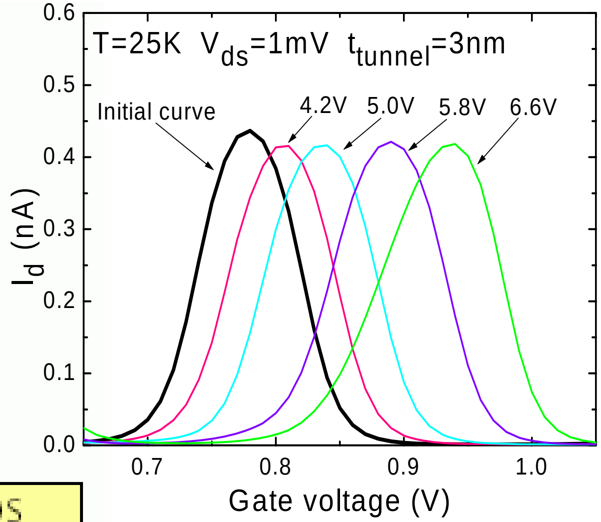


Largest CB Oscillations at room temperature!

K. Miyaji et al. , Applied Physics Letters, 143505, 2006.

Application to Analog Pattern Matching

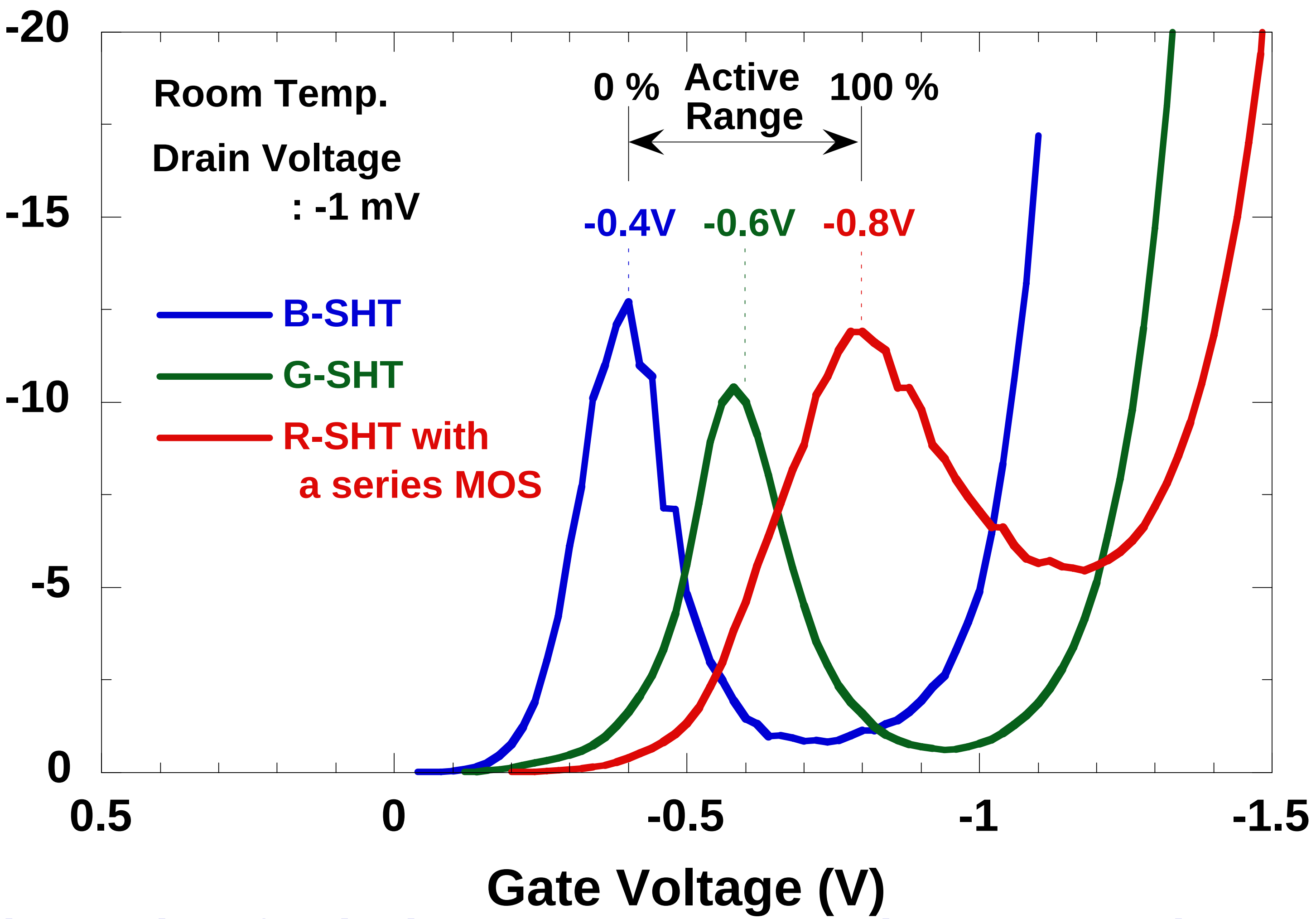




Courtesy: Prof. T. Shibata, University of Tokyo

The input image and storage data are compared in pattern matching. The 2D data are translated into 1D data to simplify the processing.

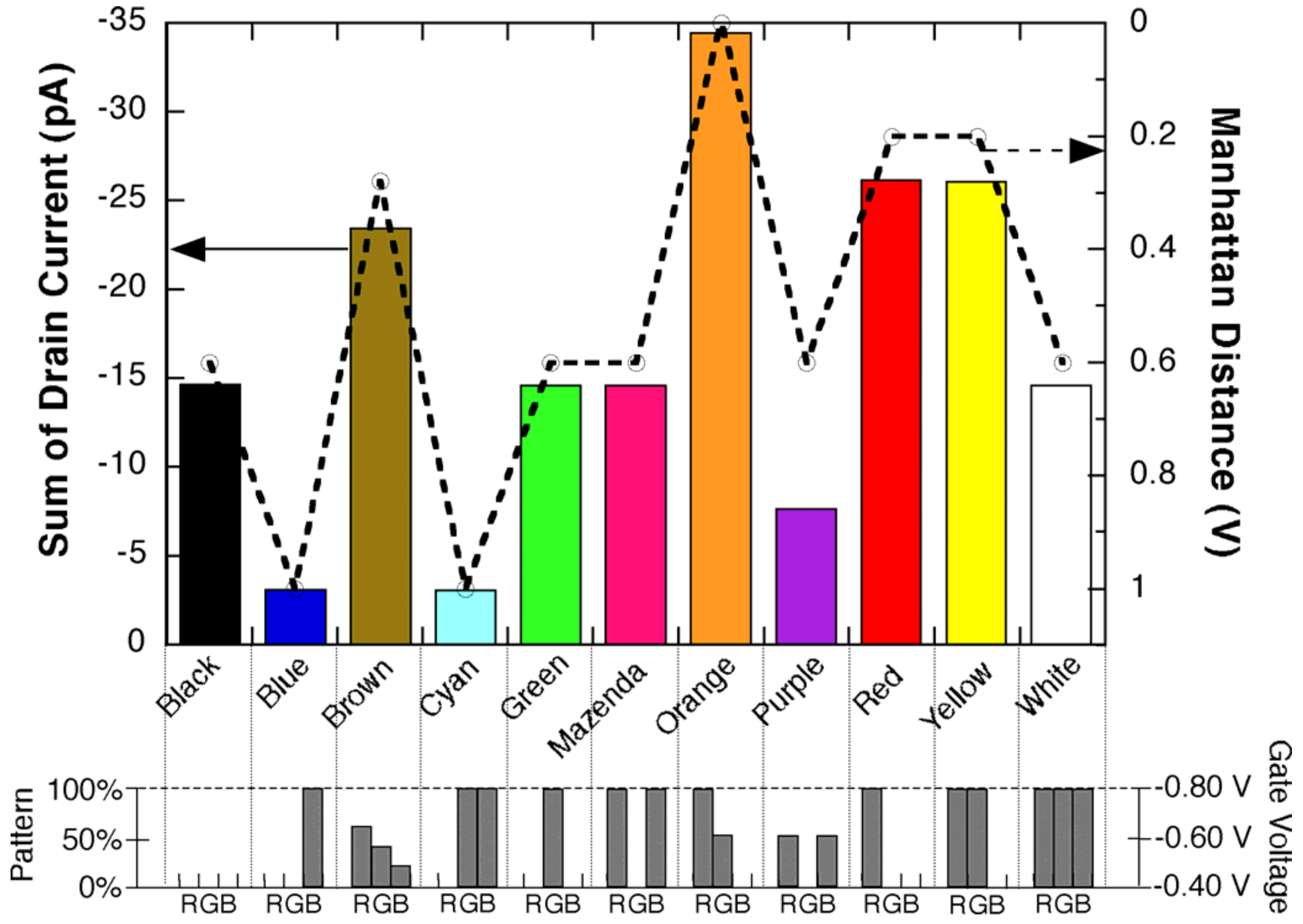
Integration of Three SETs



The peaks of 3 devices are programmed to 0, 50, and 100%.
Then, "orange" are stored in memory.

M. Saitoh et al., IEDM, p. 187, 2004

Reading (Sum of the Current)



The output current reflects the similarity between input and "orange". The output is the largest when "orange" is input.

M. Saitoh et al., IEDM, p. 187, 2004.

Summary

1. "CMOS Extension" is the most important
   - New transistor structure
   - New materials
   - Variability

2. Future Silicon Nanoelectronics
   - Fusion of More Moore, More Than Moore, and Beyond CMOS.