

Japanese Government Funding Nanoelectronics Projects

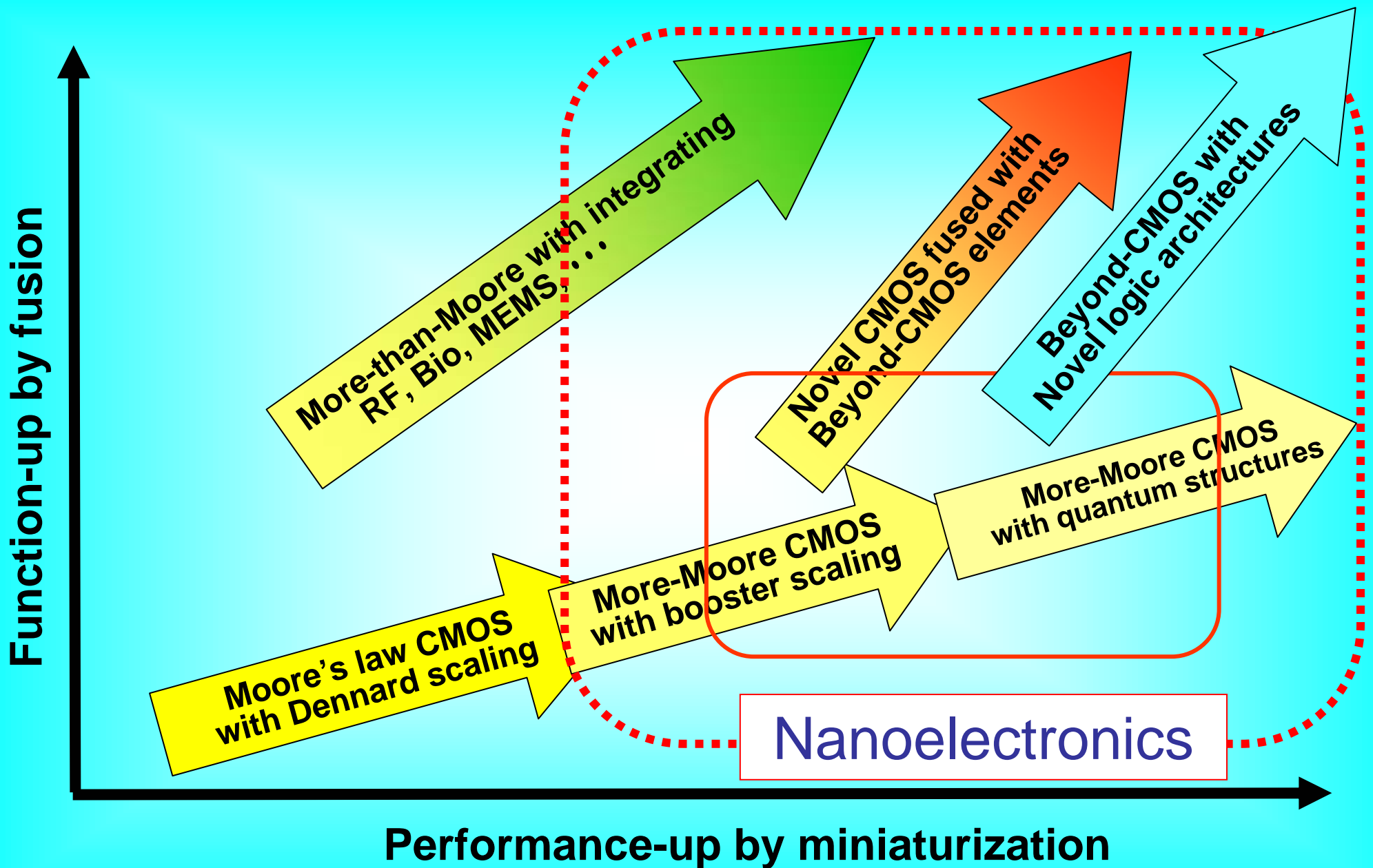
- METI
 - MIRAI project
 - Nanoelectronics projects
- MEXT
 - CREST project
 - Post scaling Si-Nanoelectronics project

Hisatsune Watanabe

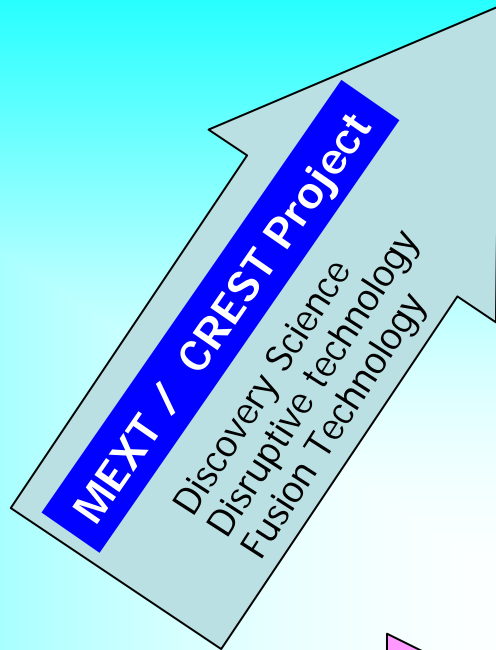


CREST

METI : Ministry of Economy, Trade and Industry
MEXT: Ministry of Education, Culture, Sports,
Science and Technology



Nanoelectronics projects supported by Government



Discovery Science (DS)

After deep scientific study, novel principle or concept is hoped to be discovered, and related application will be proposed.

Disruptive Technology (DT)

Very novel and attractive, but some drawback is pointed out, but eventually it is expected to become a main stream technology with replacing conventional ones.

Fusion Technology (FT)

Novel application development using novel devices by fusing "Beyond CMOS" elements into CMOS LSI

METI / MIRAI project
Booster scaling CMOS devices

METI / Nanoelectronics Project

Nano CMOS devices

MEXT / Post scaling Si Nanoelectronics Project

Underlying science of Nano Si CMOS devices

Performance-up by Miniaturization

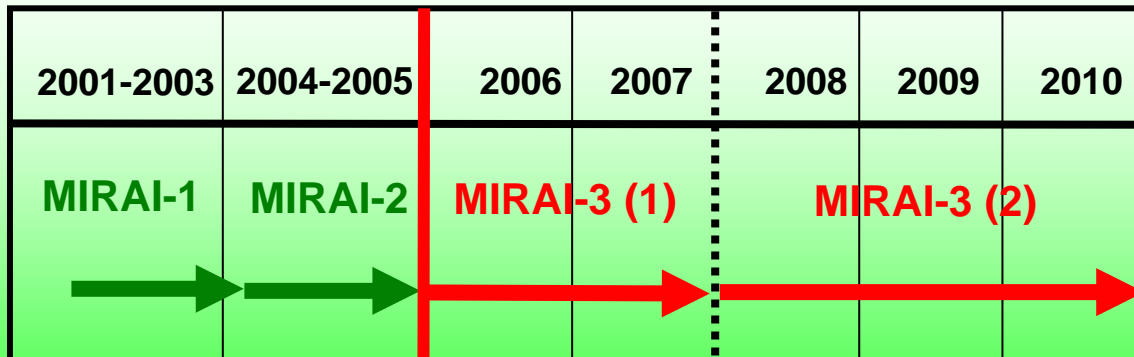
Development of basic core technologies of high performance and low power consumption system LSI for Information Society

MIRAI - 1 : Core technologies around hp65nm

MIRAI - 2 : Core technologies around hp45nm

MIRAI - 3 : Core technologies beyond hp45nm

Project Leader : H. Watanabe (Selete)



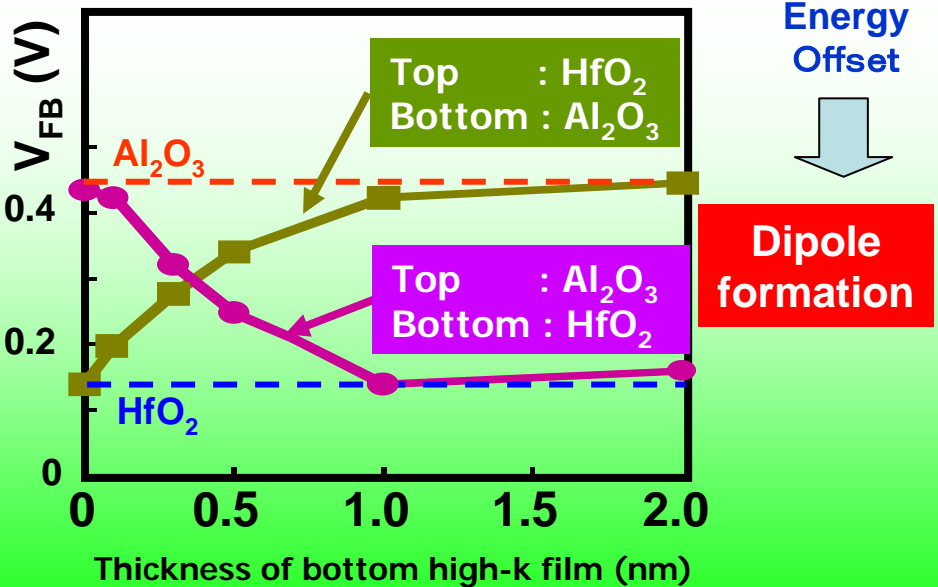
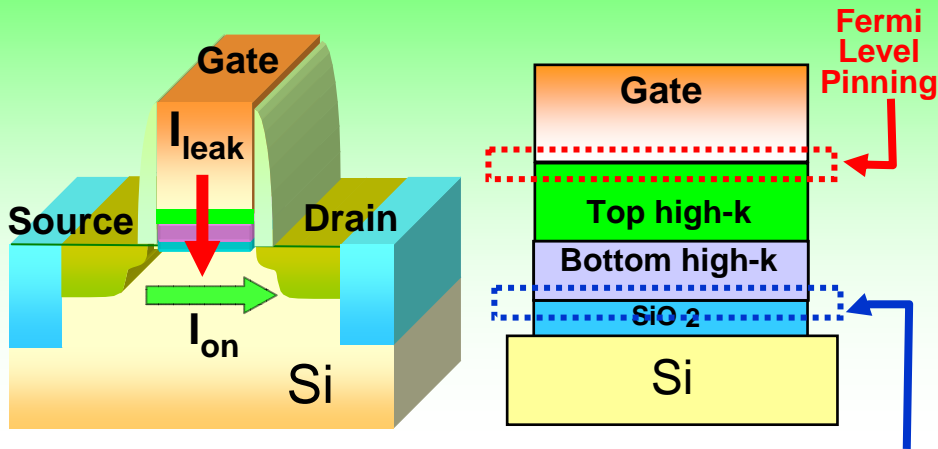
MIRAI-3 Research theme

- **Ultra-scaled CMOS**
 1. New structure transistors
 2. Ultimately thin gate stack

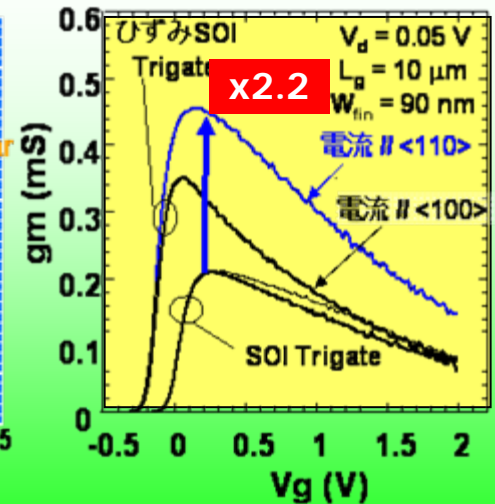
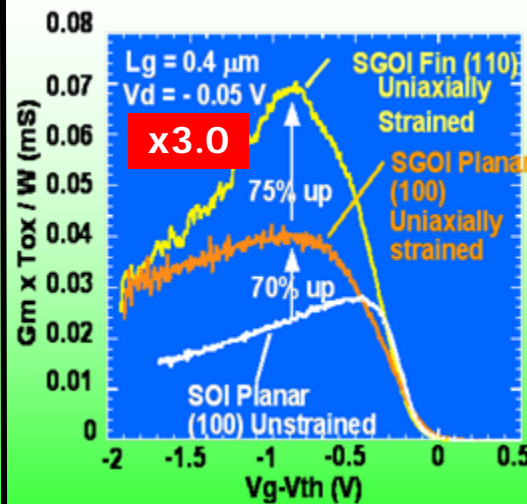
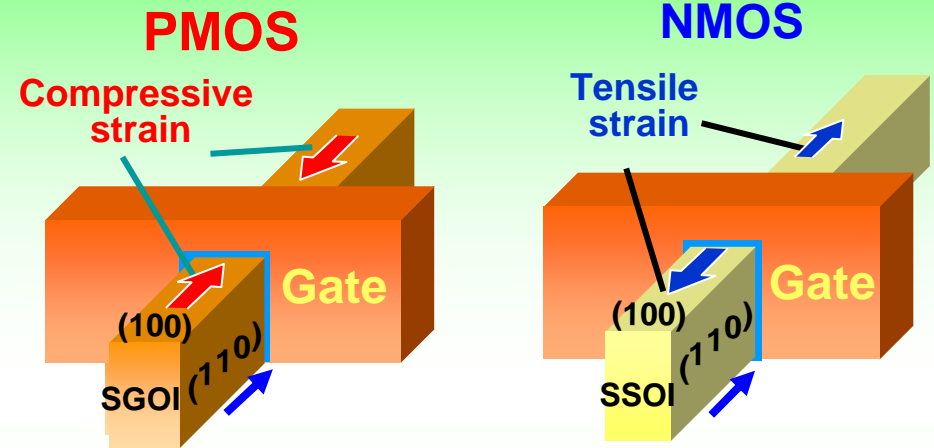
- **Nano Silicon Integration**
 3. Robust transistors
 4. SET tolerant devices
 5. CNT interconnect
 6. Optical interconnect

- **EUVL**
 7. Mask core technology

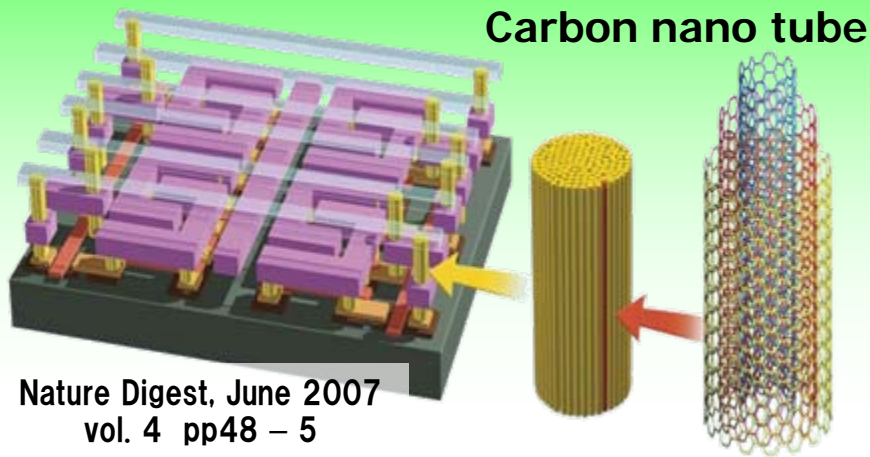
Ultra thin gate stack for increase of I_{on}/I_{leak}



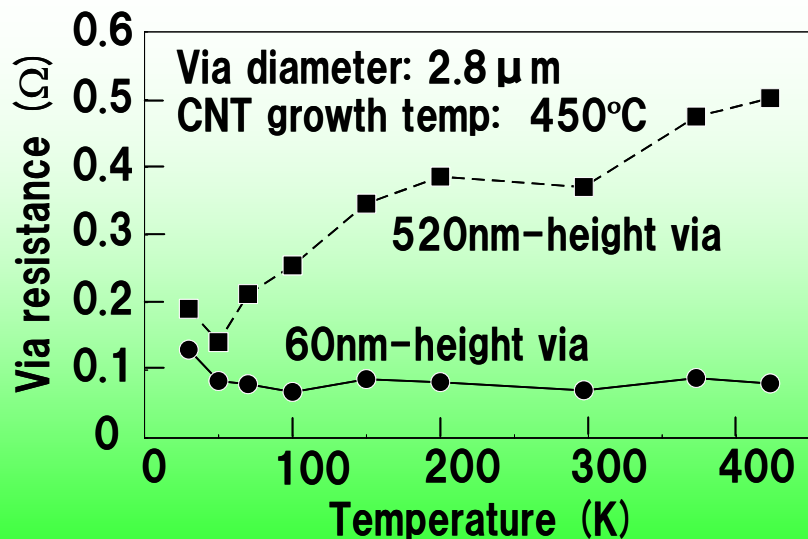
Multi-gate CMOS for large drivability



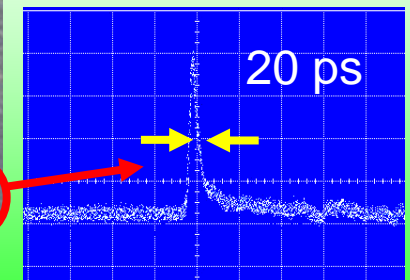
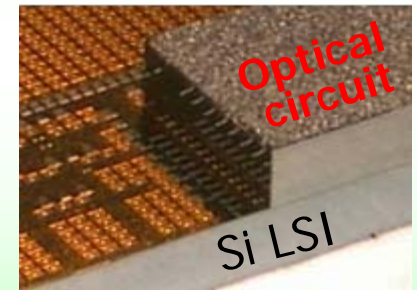
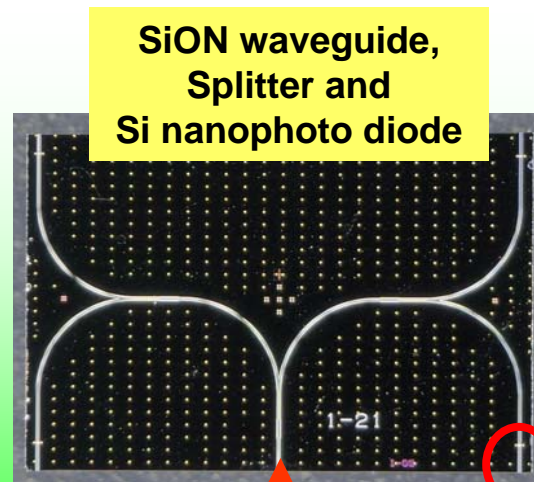
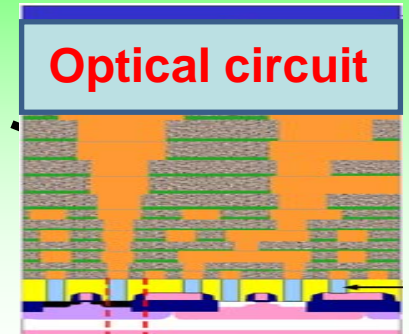
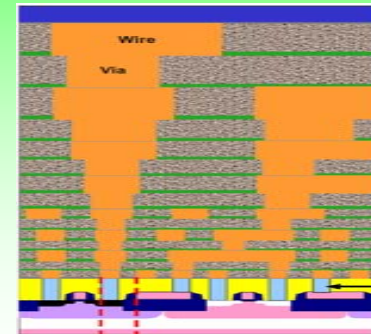
Post- Cu via using CNT for Electro Migration tolerant interconnect



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vol. 4 pp48 - 5

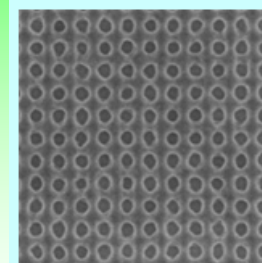


Optical interconnect for high speed, low noise and low power

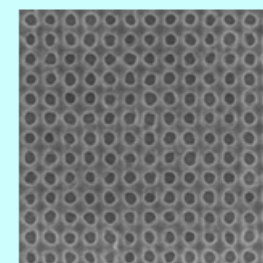


Optical input

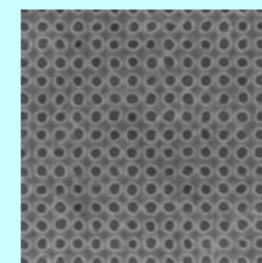
METI/NEDO MIRAI project : EUV Lithography



40 nm C/H



35 nm C/H



32 nm C/H



hp 45 nm SRAM パターン Cell size = 0.191 mm²

Isolation
 Contact
 Gate
 Interconnect

Novel materials and structures of Nanoelectronics semiconductor

Virtual research organization

Advisory Board (Chair : Prof. T.Sugano)

A-Group : Silicon Nano-wire transistors

1. Head : H. Iwai TIT
2. Head : T. Hiramoto (Tokyo Univ.)
3. Head : T. Kanayama (AIST)

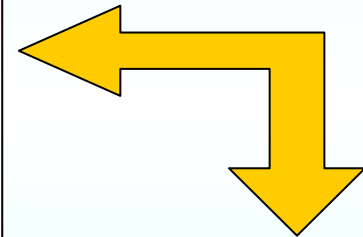
B-Group : Memory

1. Head : J. Tominaga (AIST)
2. Head : T. Wada (AIST)
3. Head : H. Yamada (Kyoto Univ.)

C-Group : Emerging Research Materials

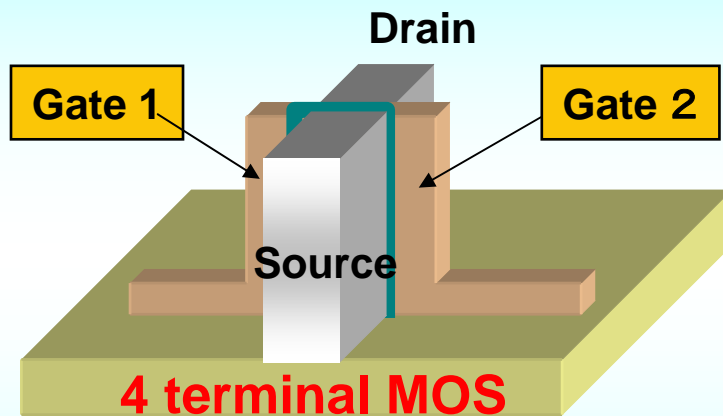
1. Head : S. Takagi (Tokyo Univ.)
2. Head : T. Mizutani (Nagoya Univ.)
3. Head : T. Goto (Niigata Univ.)

Collaboration



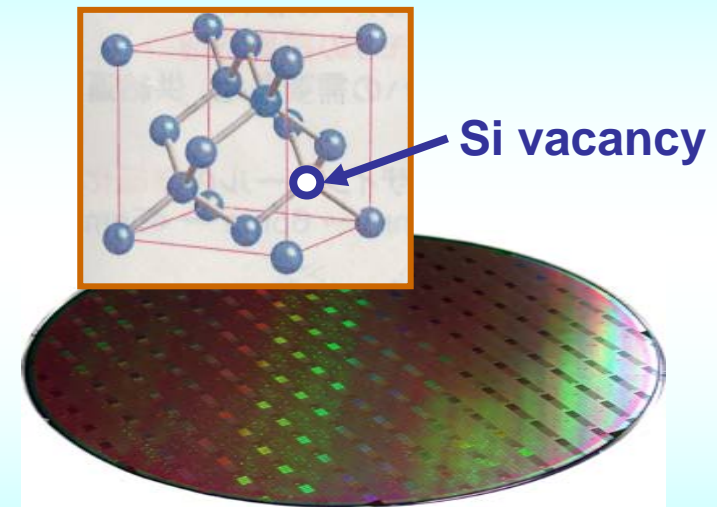
**MEXT/JST
CREST
(H. Watanabe)**

**Development of new structure
MOS transistor for ultra-low
power and noise-tolerant LSI**



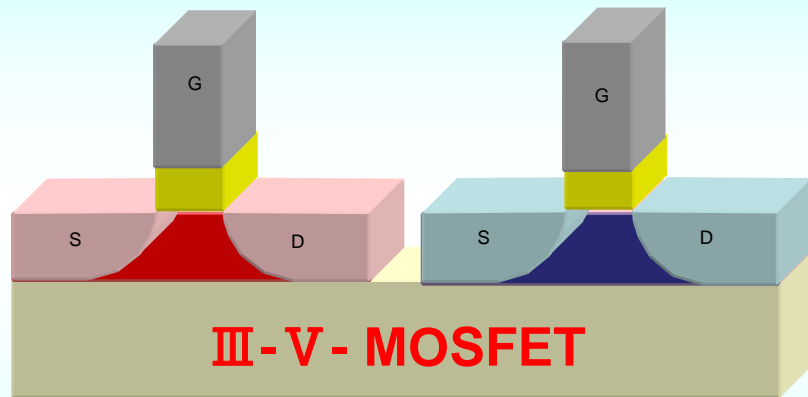
• AIST

**Development of Si vacancy
concentration measurement
by using ultrasonic wave**



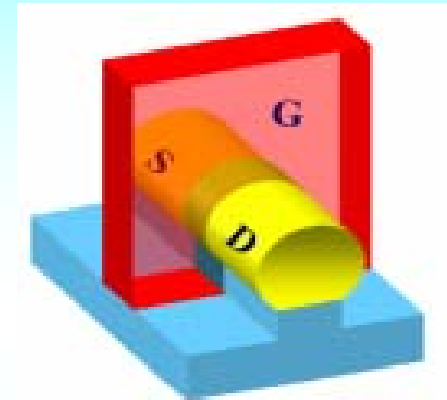
- Niigata University
- Covalent Materials Corporation
- Toshiba Corporation

Development of III-V MOSFET and III-V-On-Insulator MOSFET



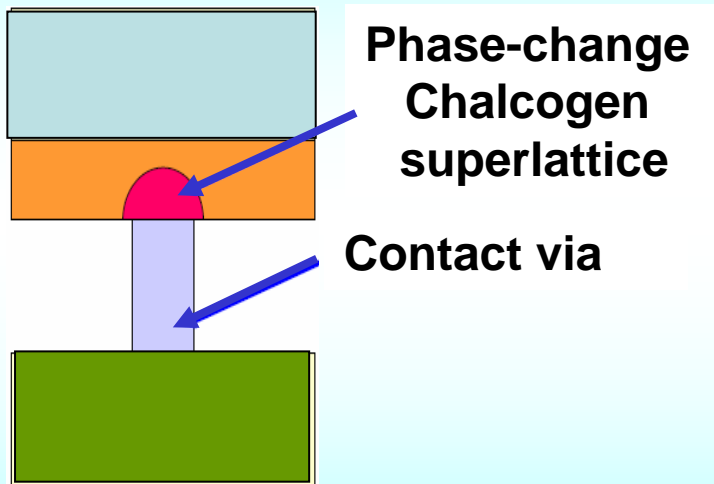
- Tokyo University
- AIST
- NIMS
- Sumitomo Chemical Corporation

Nano-wire Silicon and CNT transistors



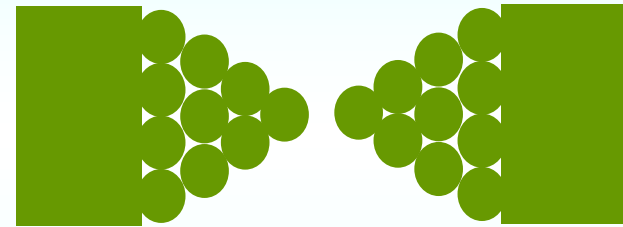
1. AIST
2. Tokyo Institute of Technology
Tsukuba University,
Waseda University
3. Tokyo University, Toshiba Corp.
4. Nagoya University

Phase change memory using a novel phenomenon of chalcogen superlattice phase change



- AIST

Non-volatile memory using metal nano gap



Metal nano gap

- Kyoto University
- AIST
- Funai Electric Corporation

MEXT/JST CREST Project

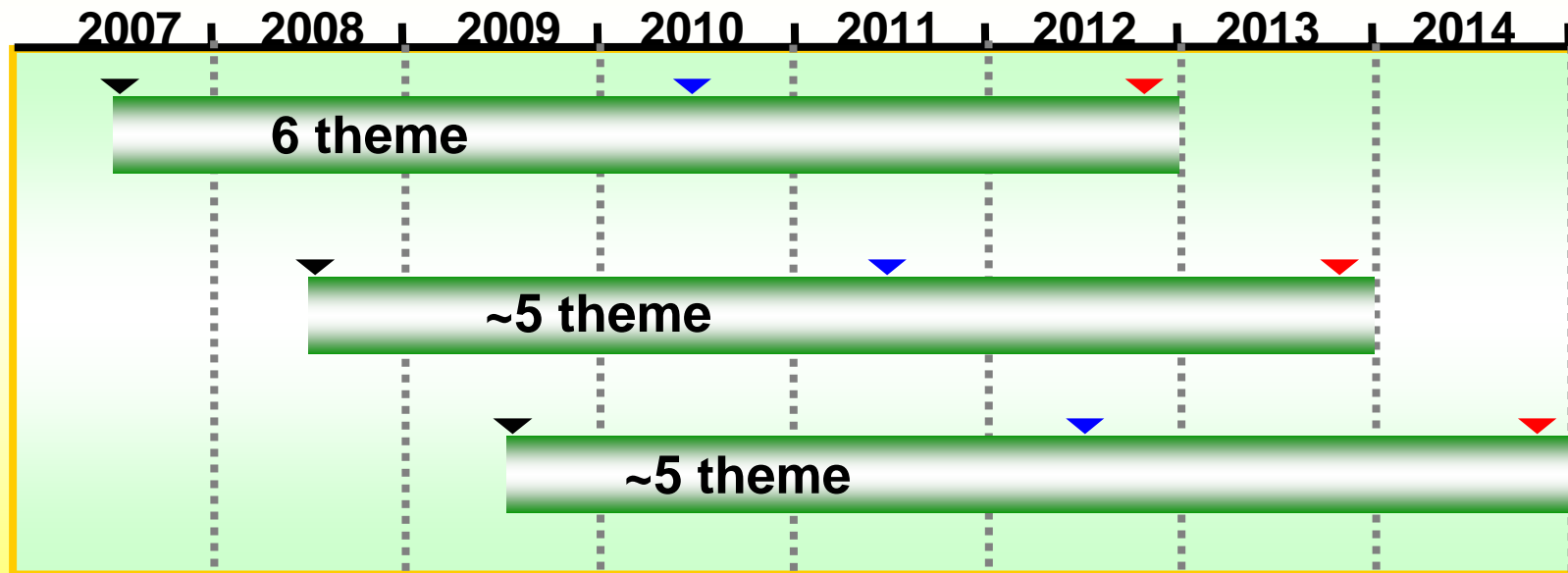
MEXT
Strategic Sector

Exploitation of materials and nano-processes for realization of novel devices with novel concepts, novel functions and novel structures

JST
Research area

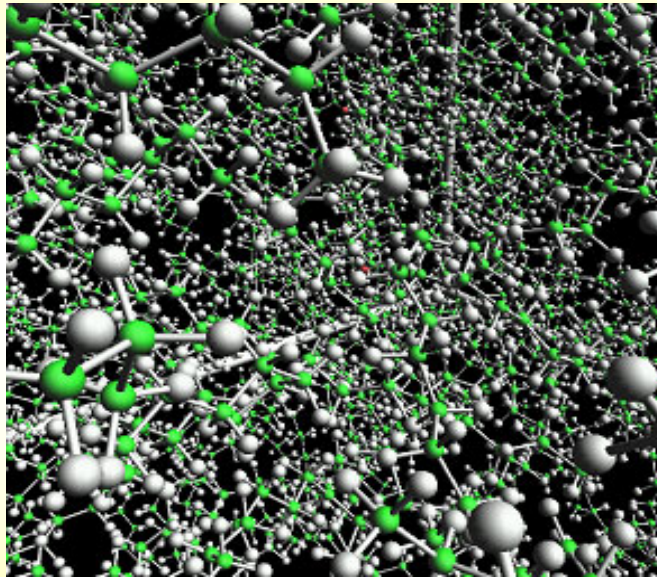
Research of Innovative Material and Process for Creation of Next-generation Electronic devices

Research supervisor H. Watanabe (Selete)



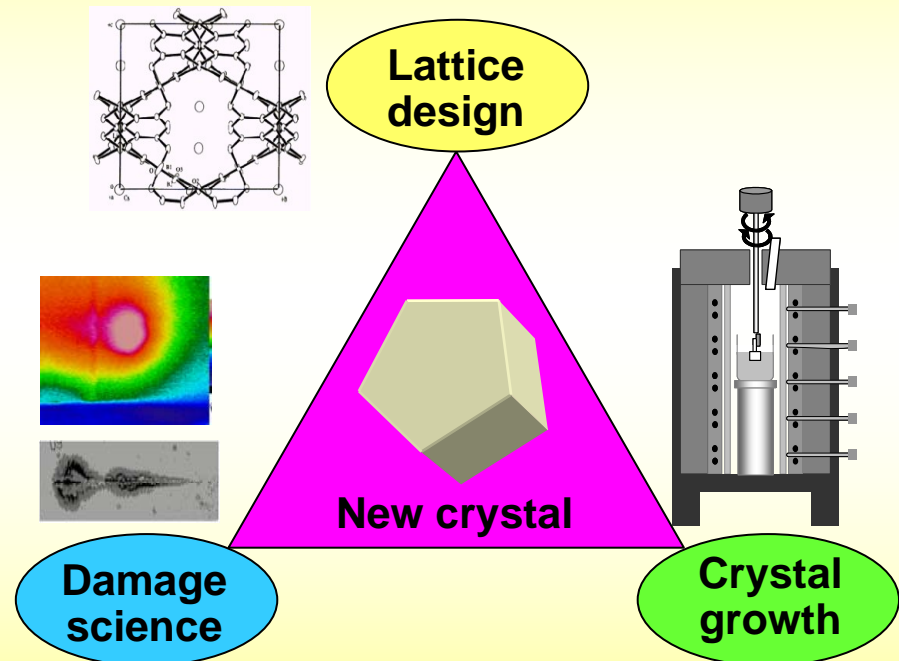
<http://www.jst.go.jp/kisoken/crest/>

Nano-chemistry science of resist material to find a solution of resist tri-lemma problem



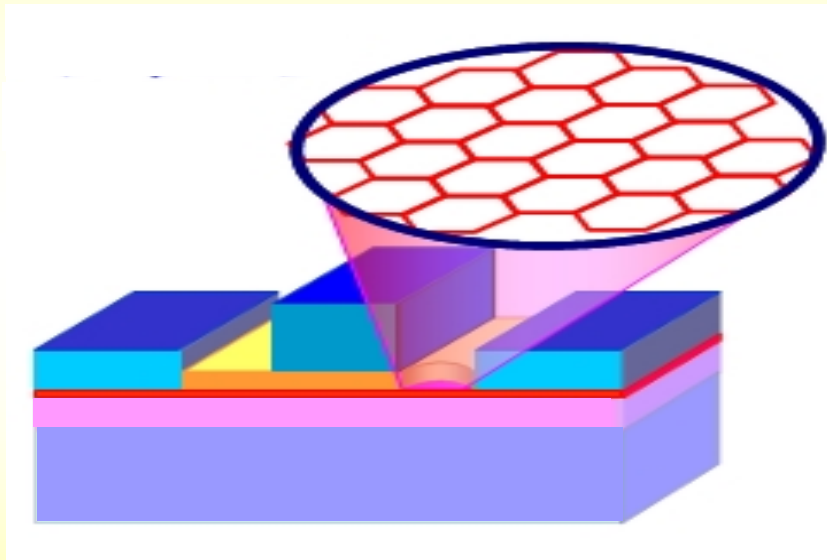
**The Institute of Scientific and Industrial Research
Osaka university**

Non-linear optical crystal development for next generation VUV laser for nano-inspection



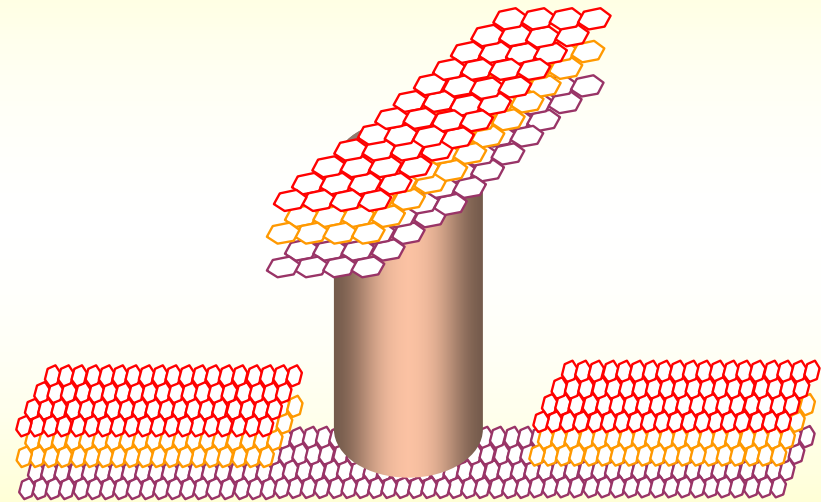
**Frontier Research Center
Osaka University**

Material and device development of complementary Graphene-on-Silicon (CGOS)



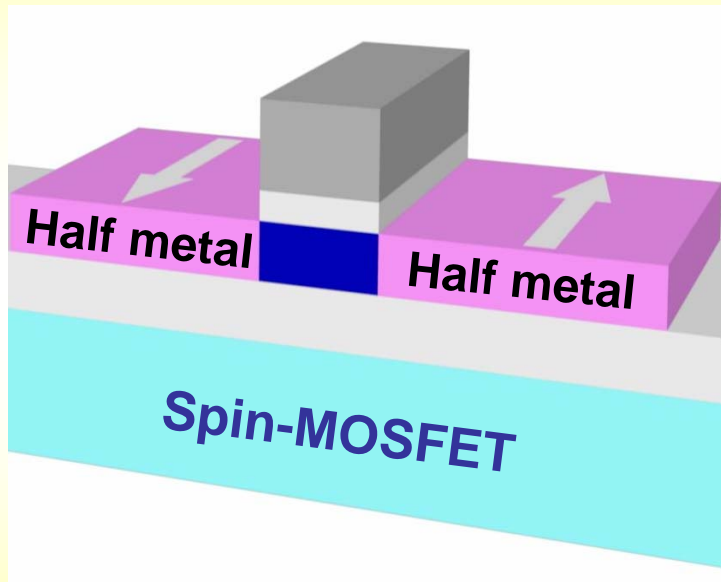
**Research Institute of Electrical
Communication
Tohoku University**

**3D active interconnect development
using graphene ribbons and FETs**



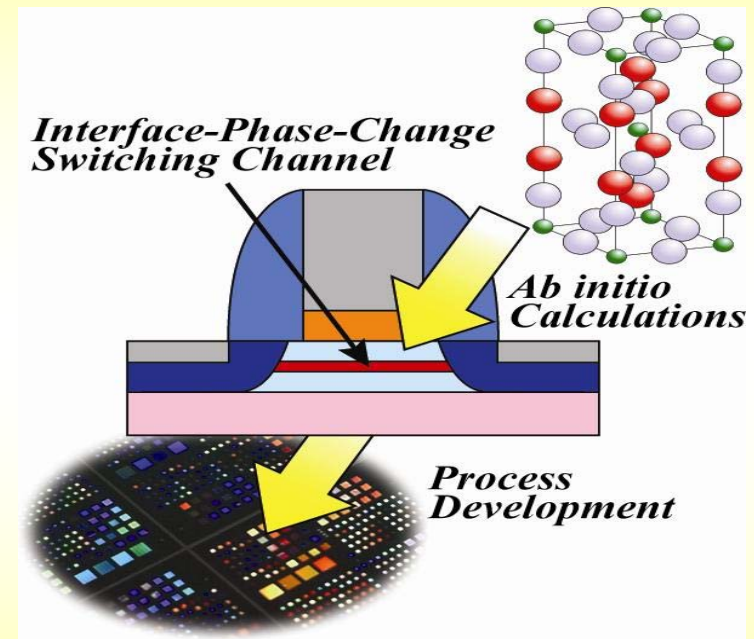
Fujitsu Ltd.

Reconfigurable spin MOSFET using half-metal ferromagnetic material



Tokyo Institute of Technology

Nonvolatile CMOS development using interface-phase-change functional oxide



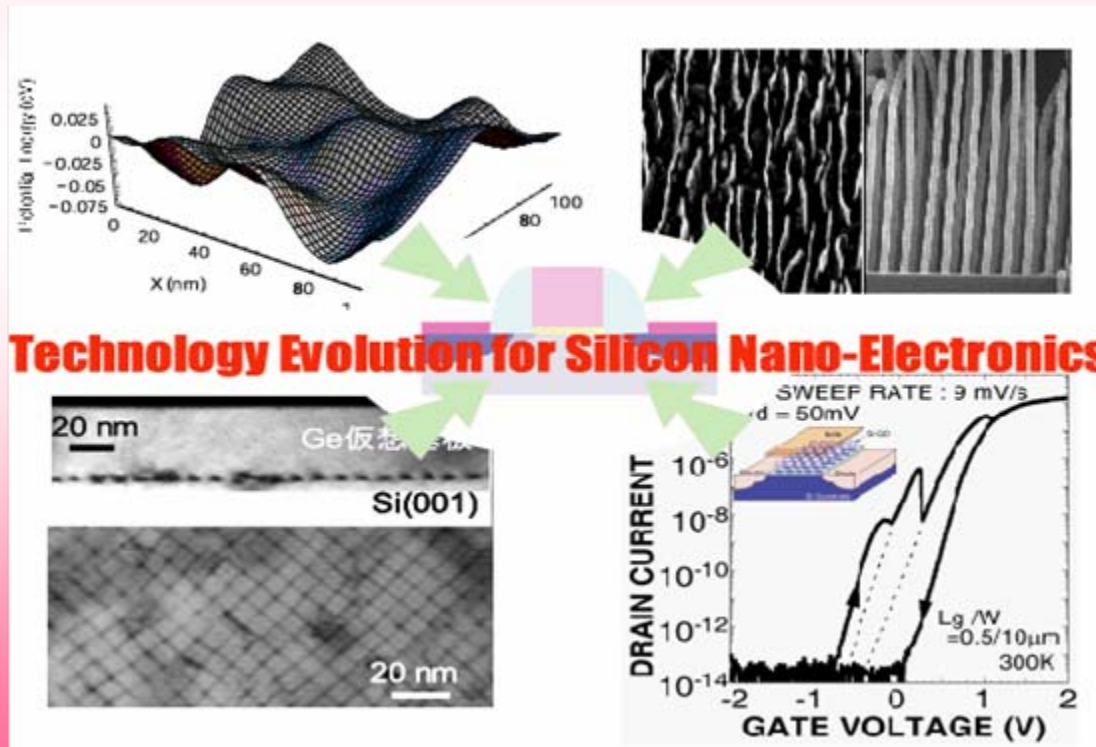
Nanotechnology Research Institute
AIST

Grant-in-Aid for Scientific Research on Priority Areas

Technology Evolution for Silicon Nano-Electronics - Post-Scaling Technology -

Head Investigator: Shigeaki Zaima (Nagoya University)

- Project : 2006-2009
- 4 research Areas (A1,A2,A3,A4)
- 18 research Groups



New Materials

- Ge, Strained Ge
- Graphen sheets
- Transition metal oxide
- Rare-earth metal oxide...

New Processes

- Radical control process,
- Bio-mineral process
- Dislocation structure control
- ...

New Device Structure

- Thin-GOI, SGOI
- Floating-dot gates
- Fin FETs
- ...

